Specification

for

micro QUAD SMALL FORM-FACTOR PLUGGABLE FOUR CHANNEL PLUGGABLE TRANSCEIVER, HOST CONNECTOR, & CAGE ASSEMBLY FORM FACTOR

Rev 2.5 September 11, 2017

Abstract: The micro QUAD SMALL FORM-FACTOR PLUGGABLE (microQSFP) specification defines requirements for a form factor supporting up to four electrical channels, high system density, and a high performance thermal solution. Support for 28 Gb/s signal rates on each channel enables many applications including 10 Gigabit Ethernet, 25 Gigabit Ethernet, 50 Gigabit Ethernet, 100 Gigabit Ethernet, 16GFC, 32GFC, and 128GFC, where higher densities are required than are possible with existing form factors. Included are definitions of electrical, mechanical, and management interfaces, electrical connector, guide rail (cage), front panel and host PCB layout, and optical connector options. By addressing the thermal, signal integrity, electromagnetic, and electrostatic challenges of a high density solution, the microQSFP Specification enables higher density networking solutions that are critical to support the continuing network demand.

This document provides a common specification for systems manufacturers, system integrators, and suppliers of modules.

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EXPRESSION OF SUPPORT BY MANUFACTURERS

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MultiLane SAL
Oclaro, Inc.
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Change History:

Revision	Date	Changes
1.0	January 14, 2016	-First Public Release, released as Draft Mechanical Only Specification.
2.0	March 17, 2016	-Second Public Release, released as Complete MSA Specification -Various editorial changes to text, figures, and tables. -Contributor members added, Amphenol, Finisar, Lorom, MulitLane SAL, Oclaro, Inc, Rosenberger, and Semtec. -Table of contents updated. -Content of Clause 4 content moved to Subclause 4.1. -Content added in Subclause 4.1, including text prior to figure 1, and table 1, figure 2a, figure 2b and content after figure 1. -Contact 31 changed from TBA* to VccMgmt in figure 1. Contact defined in detail in Subclauses in Clause 4. -Subclauses 4.2, 4.3, 4.4, 4.5, and 4.6 created. Includes all text, items, table 2, table 3, & Figure 3 -Table 2 is now Table 4. Listed figures in table 4 updated to reference new figure numbers. -Figures 3, 4, 5, 6, 7, 8, 9, 10, 11, & 12, are now figures 5, 6, 7, 8, 9, 10, 11, 12, 13, & 14 respectively. -RFS Symbol removed from all feature control frames found in the figures 6, 7, 8, 9, 12, & 13. -Contact numbers identified in figures 6, 7, 9, & 12. -In figure 8, 2X 40.84 BASIC added, Keepout zones identified. -In figure 9, LMC changed to MMC on feature control frame associated with 1.05 hole identifying datum J. -In figure 12, rear of connector enlarged, dim 11.75 from datum L was 9.95, and dim 6.75 -Content from clause 6 moved to Subclause 6.2, and content of Subclause 6.1 created including table 6. -Clause 7 (Management Interface) content created.

2.1	May 26, 2016	-Various editorial changes to text, figures, and tables. -Contributor member added, MACOM. -Table of contents updated. -Subclause 4.3.2 updated with reference to Subclause 7.3.10. -Extended Identifier Table 8 created, placed in Subclause 7.2.1. Table numbers re-ordered after Table 8. Subclauses 7.2.2 and 7.2.3 continue after inserted Subclause 7.2.1. -DataPathInit duration clarified in Subclause 7.3.3. -TX_TurnOn duration clarified in Subclause 7.3.5. -2 Second Timeout Removed from Figures 15 & 16, all timing placed in new Table 12 in Subclause 7.3.10
2.2	June 03, 2016	-Third public release. -Various editorial changes. -Replaced Page 03h Byte 252 with Lower Memory Byte 114 in all instances.
2.3	September 09, 2016	-Fourth public release. -Figure 6 dimension changes as follows: 44.1 MAX internal depth of note 6 was 44 MAX, 9.2 distance from latch to cage stop was 9.1, 15.9 MAX distance from cage stop to front of module was 16 MAX. -Figure 7 dimension changes as follows: (2.6) contact point distance was (2.5), 3.1 distance front edge of module card to edge of pad was 3.
2.4	January 13, 2017	-0111b in Table 10 now assigned to 1 to 5 seconds, all subsequent times shift down 1 row in table 10. -Clause 8, Appendix A was created. Appendix A covers interface definitions for modules and connectors that support PCIe applications.
2.5	August 28, 2017	-Figures 2 & 3 and supporting detail added in Subclause 4.1, for single and two channel modules positions. -Figures re-numbered starting with figure 4. -Clause 9.0 Appendix B for 1, 2, & 4 Channels added.

TABLE OF CONTENTS

1. Scope

This specification defines the electrical, management, and optical interfaces, the mechanical form factor, thermal requirements, EMI, and ESD requirements for a 1, 2, or 4-channel (such as 28 GBd per channel) transmit/receive hot-pluggable module, connector, and cage. Clause 3 defines these items in more detail.

1.1 Description of Clauses

Clause 1 contains the Scope and Purpose

Clause 2 contains Referenced and Related Standards and Specifications

Clause 3 begins the specification

Clause 4 contains electrical specifications

Clause 5 contains mechanical specifications and printed circuit board recommendations

Clause 6 contains thermal considerations

Clause 7 is a description of the management interface and management register contents.

Clause 8 is Annex A defining signal symbols and contact numbering for PCIe applications

Clause 9 is Annex B showing examples of 1, 2, 4 channel and breakout applications

2. References

The microQSFP MSA activities support the requirements of the networking, computing, and storage industries.

2.1 Industry Documents

The following interface standards and specifications are relevant to this Specification.

- GR-253-CORE
- IEEE Std 802.3-2015
- IEEE Std 802.3by 25 Gb/s Ethernet, amendment to 802.3-2015
- IEEE Std 802.3cd 50Gb/s, 100Gb/s, 200Gb/s Ethernet, Draft amendment 802.3-2015
- InfiniBand Architecture Specifications FDR, EDR and draft HDR
- FC-PI-5, FC-PI-6, FC-PI-6P
- FC-PI-7 64GFC/256GFC Project
- SAS 4.0
- Optical Connectors: MPO: IEC 61754-7, Dual LC: IEC 61754-20
- Aligned key (Type B) MPO patch cords: TIA-568
- Dual LC optical patch cord: NEBS GR-63
- SFF-8665 QSFP+ 28 Gb/s 4X Pluggable Transceiver Solution (QSFP28)
- SFF-8636 Management Interface for Cabled Environment (Revision 2.9)
- SFF-8679 QSFP28 4X Base Electrical Specification (Revision 1.7)
- PCI Express External Cabling Spec (Revision 3.0, Version 0.7)
- 25G 50G Ethernet Consortium, Schedule 3 Specification, Rev. 1.6

2.2 SFF Specifications

A possible action of the MSA is to create appropriate SFF specifications based on this MSA.

2.3 Sources

This document can be obtained via the www.microqsfp.com web site

2.4 Conventions

The ISO convention of numbering is used i.e., the thousands and higher multiples are separated by a space and a period is used as the decimal point. This is equivalent to the English/American convention of a comma and a period.

English	French	ISO
0.6	0,6	0.6
1,000	1 000	1 000
1,323,462.9	1 323 462,9	1 323 462.9

3. Introduction

This Specification covers the following items:

a) Electrical interfaces (including contact assignments for data, control, status, configuration and test signals) and the electrical Connector and recommended host PCB layout.

b) Management interfaces encompassing features from the current QSFP28 SFF documents and includes support for multiple physical media (copper, optics etc), specific multi-data rate and multi-protocol implementations.

c) Optical interfaces including the optical Connector receptacle and mating fiber optic Connector plug and recommended breakout cable assembly. The optical specifications are left to the applicable standards for each protocol.

d) Mechanical definitions including package outline with latching detail and optical Connector receptacle detail, electrical Connector mechanical details for both the Module and host PCB halves, front panel cut-out recommended dimensions.

e) Thermal requirements and considerations.

f) Electromagnetic interference (EMI) recommendations, including necessary shielding features to seal the OEM chassis front panel output with and without the microQSFP Module installed in the Cage.

g) Electrostatic discharge (ESD) requirements solely to the extent disclosed in the Specification where the sole purpose of such disclosure is to enable products to operate, connect or communicate as defined within the Specifications.

The Specifications will provide a common solution for combined four-channel ports that support OTN and/or Ethernet and/or InfiniBand and/or Fibre Channel specifications. This specification encompasses design(s) capable of supporting multimode, single-mode Modules, passive copper, active copper, and active optical cables. Electrical and optical specifications may be compatible with standards under development.

4. Electrical Specification

This microQSFP Specification adopts the compliance electrical and timing requirements found in Clauses 4, 5, and 8 of SFF-8679 except as noted here in Clause 4. The scope of SFF-8679 includes: electrical contacts for the host Connector, fiber positions for optical interfaces, power supply requirements, ESD, and thermal characteristics of pluggable modules and direct attach cables. Any exceptions to SFF-8679 will be defined in this specification.

4.1 Electrical Interface

Electrical Interface and connector definitions of SFF-8679 Rev 1.7 Subclause 5.1 are replaced by this Subclause 4.1. Figure 1 shows the signal symbols and contact numbering for the microQSFP Module edge Connector. The diagram shows the Module PCB edge as a top and bottom view. There are 38 contacts intended for high speed signals, low speed signals, power, and ground connections. Table 1 contains the microQSFP Module Electrical Interface Map.

The module contains a printed circuit board that mates with the electrical connector. The pads are designed for a sequenced mating:

First mate - ground contacts
Second mate - power contacts
Third mate - signal contacts

For EMI protection the signals to the connector should be shut off when the module is removed. Standard board layout practices such as connections to Vcc and GND with Vias, use of short and equal-length differential signal lines, use of microstrip-lines and 50 Ohm terminations are recommended. The chassis ground (case common) of the module should be isolated from the module's circuit ground, GND, to provide the equipment designer flexibility regarding connections between external electromagnetic interference shields and circuit ground, GND, of the module.

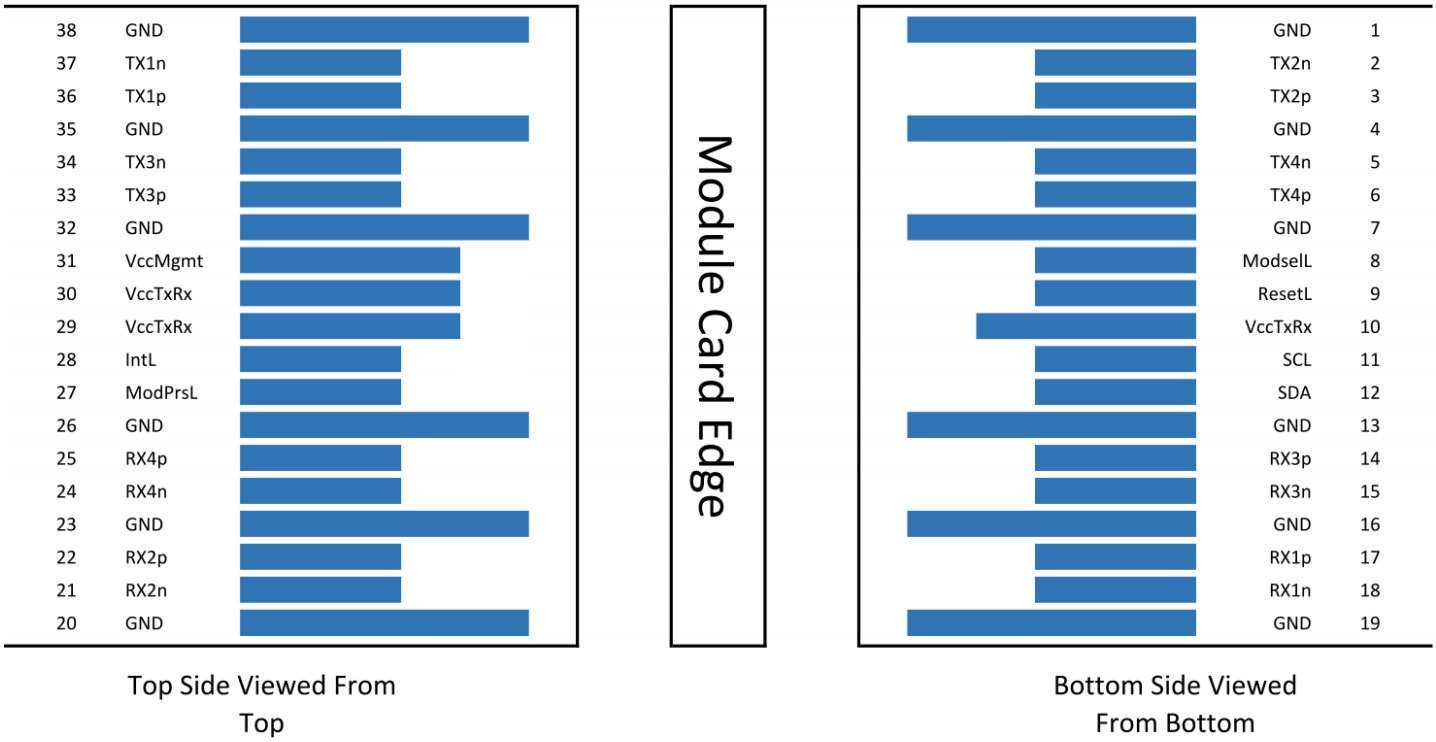

Figure 1 microQSFP Module Pad Layout

Table 1: microQSFP Module Electrical Interface Map

#	Logic	Symbol	Name	Plug Sequence	Notes
1		GND	Signal Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Signal Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Signal Ground	1	1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		VccTxRx	+3.3V Power Supply for high-speed data path ICs	2	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3	
13		GND	Signal Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Signal Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Signal Ground	1	1
20		GND	Signal Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Signal Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Signal Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL	Interrupt	3	
29		VccTxRx	+3.3V Power Supply for high-speed data path ICs	2	2
30		VccTxRx	+3.3V Power Supply for high-speed data path ICs	2	2
31		VccMgmt	Management Interface Power Supply	2	2
32		GND	Signal Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Signal Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Signal Ground	1	1

Note 1: GND is the symbol for signal and supply (power) common for the microQSFP Module. All are common within the microQSFP Module and all Module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
Note 2: Each Vcc contact is limited to maximum of 1 A. The Host shall apply power to all Vcc contacts (VccTxRx and VccMgmt) concurrently. All VccTxRx contacts may lead to a common 3.3 V Power Supply in the module. This 3.3 V Power Supply shall be electrically isolated from the VccMgmt Power Supply in the module.

4.1.1 Configurations

microQSFP has 4 electrical channels, but can support implementations with either 1, 2, or 4 electrical channels. In the 1 and 2 channel implementations, the specific electrical channels that must be used are shown in Figures 2 and 3. The un-used high speed gold mating pads on the module/cable plug card edge must still be included on the printed circuit board even in these reduced channel versions to protect the durability of the host receptacle connector contacts. In one and two channel module

implementations, the un-used gold mating pads on the module/cable plug can be left "open circuit". In all cases the microQSFP host receptacle connector is required to include all 38 contacts as shown in Figure 1. Annex B shows some example use cases for 1, 2, and 4 channel implementations used in point to point and breakout applications as well as defining the necessary memory map details for these cases.

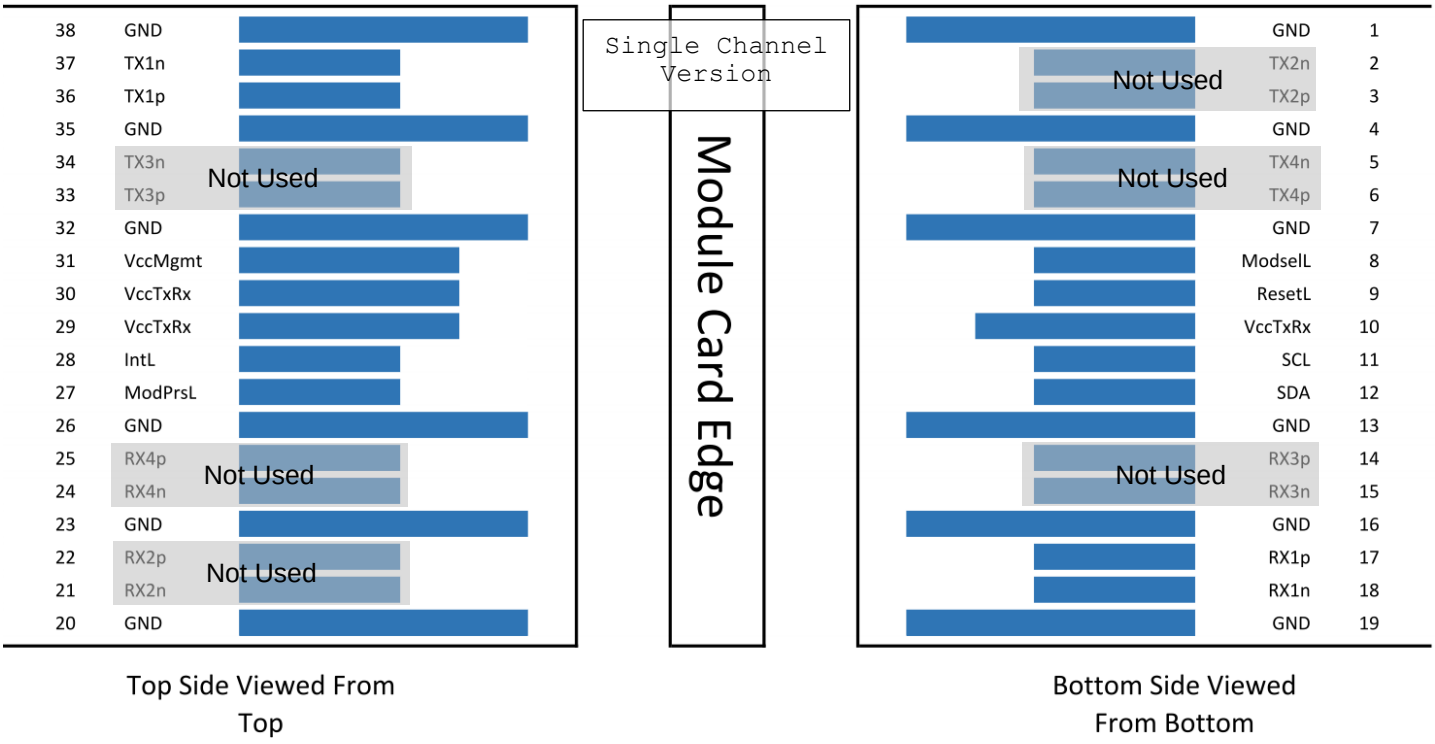

Figure 2, Single Channel Version

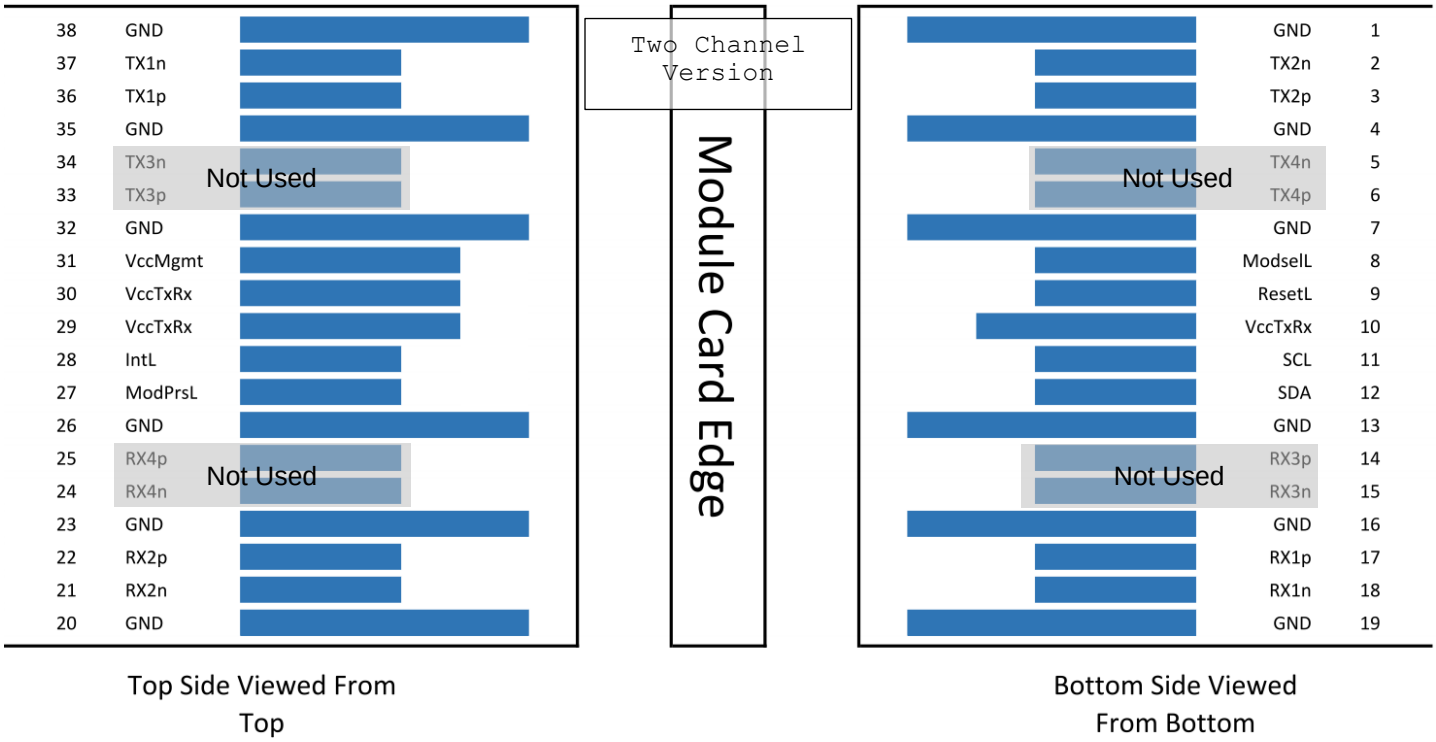

Figure 3, Two Channel Version

Figure 4 shows an example block diagram of the connectivity between the host PCB and the microQSFP module.

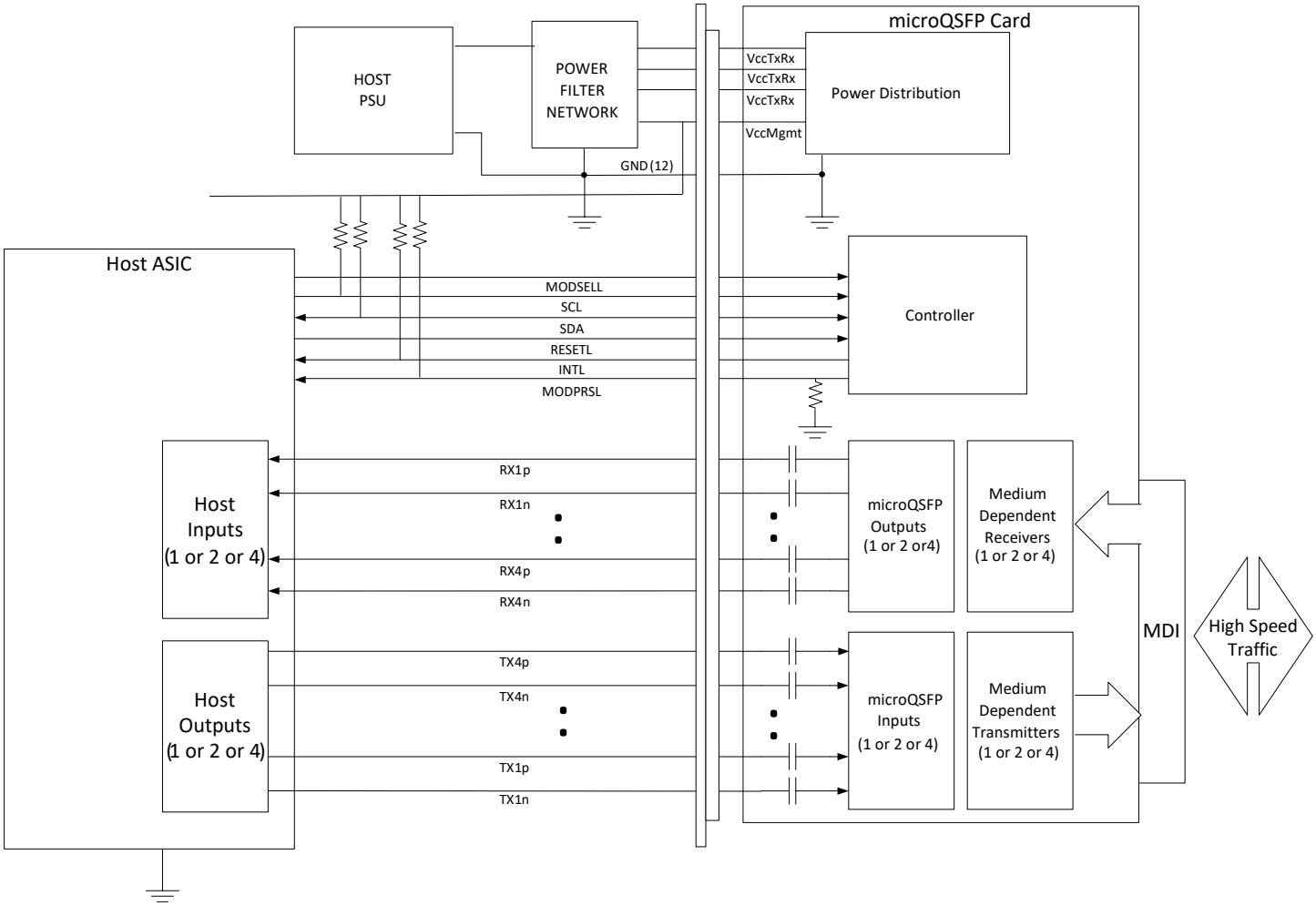

Figure 4a: Example microQSFP Host Board and Optical Module Block Diagram

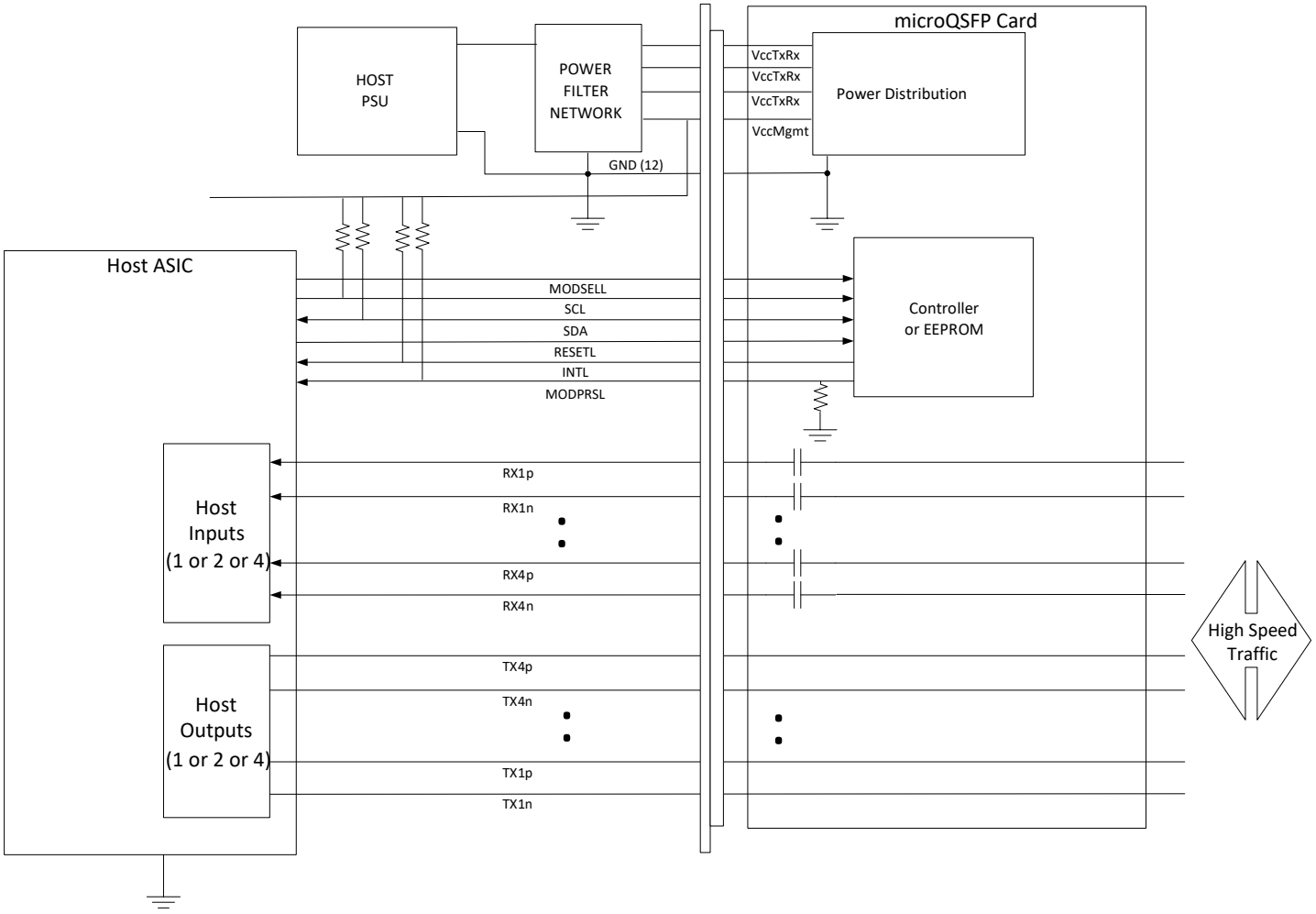

Figure 4b Example microQSFP Host Board and Copper Cable Module Block Diagram

4.2 Low Speed Signal Descriptions

Low Speed Signals are as defined in Subclause 5.2 of SFF-8679 except as follows. The signal, LPMode, has been deleted. In addition to the 2-wire serial interface the module has the following low speed pins for control and status:

ModSelL
ResetL
ModPrsL
IntL

4.2.1 ModSelL

For ModSelL see Subclause 5.2.1 in SFF-8679.

4.2.2 ResetL

For ResetL see Subclause 5.2.2 in SFF-8679.

4.2.3 ModPrsL

For ModPrsL see Subclause 5.2.4 in SFF-8679 except that in the module, ModPrsL is connected to module Signal Ground through no more than 150 Ohm.

4.2.4 IntL

IntL is as described in SFF-8679 Subclause 5.2.5

4.3 Low Speed Signal Electrical Specifications

Low speed signal electrical specifications are as defined in SFF-8679 except Subclause 4.3.1 below replaces Subclause 5.3.1 of SFF-8679.

4.3.1 Low Speed Signaling

Low speed signaling shall utilize the VccMgmt rail for all pull-ups or actively driven high signals. Hosts shall use a pull-up resistor connected to VccMgmt on each of the 2-wire interface SCL (clock), SDA (data), and all low speed status outputs. Module pullups on SCL and SDA signals are not required. If the Module implementation uses pullups on these signals, each pullup shall be at least 47k Ohms.

The SCL and SDA comprise a hot plug interface that may support a bus topology. During module insertion or removal, the module may implement a pre-charge circuit which prevents corrupting data transfers from other modules that are already using the bus.

When active modules are in low power mode, the module receiver high speed signal outputs shall be quiescent and the transmitter optical outputs shall be disabled.

Compliance with Table 2 provides compatibility between host bus masters and the 2-wire interface.

Table 2: Low Speed Signals Electrical Specification

Parameter	Symbol	Min	Max	Unit	Condition
SCL and SDA	VOL	0	0.4	V	IOL(max)=3.0mA
	VOH	VccMgmt-0.5	VccMgmt+0.3	V	
SCL and SDA	VIL	-0.3	VccMgmt*0.3	V	
	VIH	VccMgmt*0.7	VccMgmt + 0.5	V	
Capacitance for SCL and SDA I/O contacts	Ci		14	pF	
Total bus capacitive load for SCL and SDA	Cb		100	pF	3.0 k Ohms pullup resistor, max
			200	pF	1.6 k Ohms pullup resistor max
Reset and ModSelL	VIL	-0.3	0.8	V	|Iin|<=125 uA for 0V<Vin, VccMgmt
	VIH	2	VccMgmt+0.3	V	
ModPrsL and IntL	VOL	0	0.4	V	IOL=2.0mA
	VOH	VccMgmt-0.5	VccMgmt+0.3	V	

4.3.2 Low Speed Signal Timing

For exceptions and additions to Subclause 8.1 of SFF-8679, see Table 12 in Subclause 7.3.10.

All other Low Speed Signal Timing requirements are defined in SFF-8679 Subclause 5.3.2.

4.4 High Speed Signal Electrical Specifications

High Speed Signal Electrical Specifications are defined in SFF-8679 Subclause 5.4.

4.4.1 Compliance Testing

Compliance Testing requirements are as defined in SFF-8679 Clause 4 with the following exception. In Table 4-1, add to the description of TP1A, "Used to calibrate module test inputs at TP1."

4.5 Power Requirements

The following is in replacement of Subclause 5.5 in SFF-8679.

The electrical connector has three contacts labeled VccTxRx and one contact labeled VccMgmt. Each contact can concurrently support up to 1 Ampere current. The three VccTxRx contacts are in parallel and may connect to a common 3.3 V Power Supply in the module associated with the high speed signal path. The VccMgmt contact connects to a 3.3 V VccMgmt supply associated with the low speed (control) signal interface and memory. The VccTxRx supply is electrically isolated in the module from the VccMgmt supply.

The host system controls whether the module is in the low-power or high-power state via the management interface. Details of the initialization sequence are provided in Clause 7.

4.5.1 Power Classes and Maximum Power Consumption

For Power Classes and Maximum Power Consumption see Subclause 7.2.1.

4.5.2 Module Power Supply Specification

The following is exceptions and additions to Subclause 5.5.2 of SFF-8679.

Table 5-5 of SFF-8679 no longer applies. In addition the Power_Override bit and the High_Power_Class_Enable bit do not apply to microQSFP and shall be ignored by the module.

In Figure 5-5 of Subclause 5.5.2 of SFF-8679, inrush current timing is defined. The following Figure 5 is to replace SFF-8679 Figure 5-5.

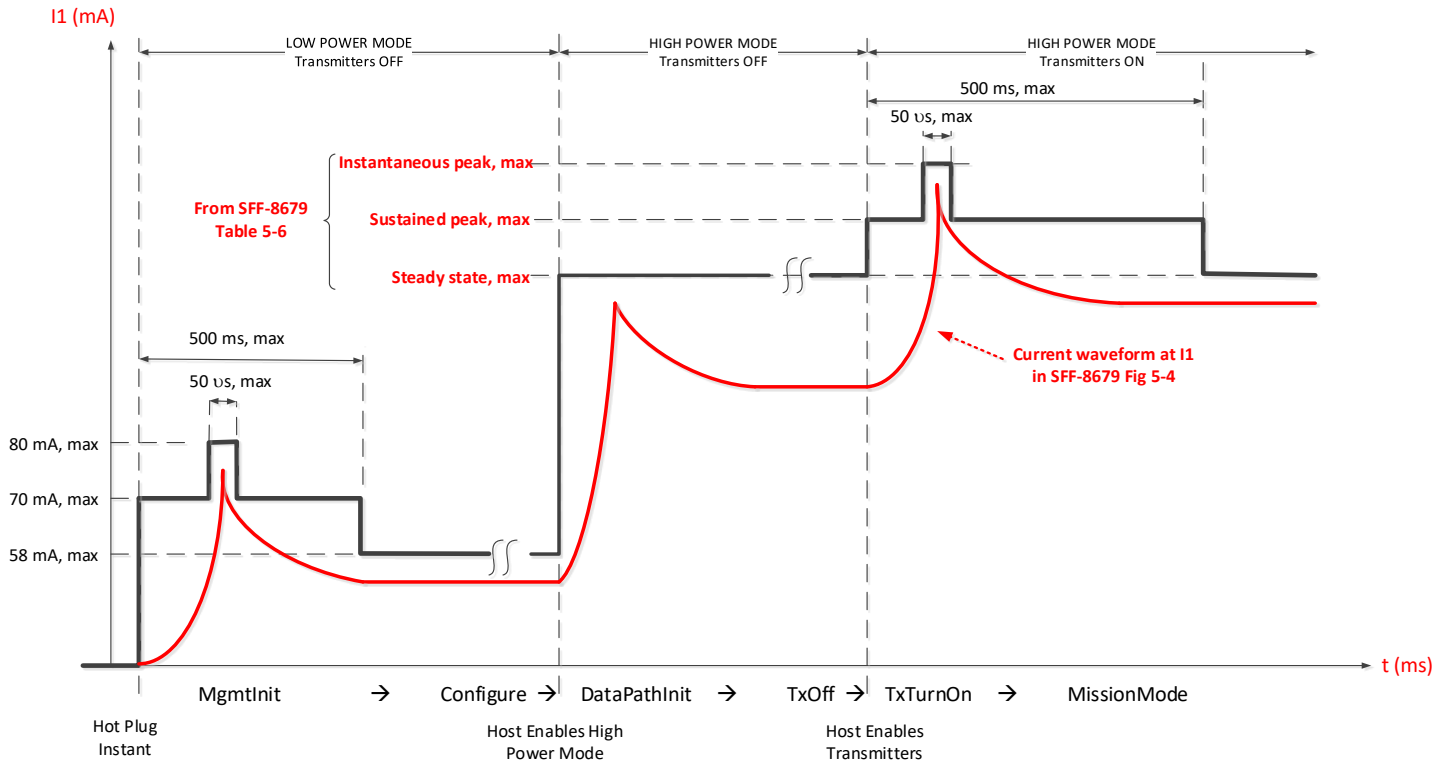

Figure 5: microQSFP Inrush Current Timing

Table 3 below is an addendum to existing Table 5-6 in SFF-8679, to define Low Power Mode operation. Additionally, the 1.5W entry for Table 5-6 shall refer only to Power Class 1

modules, not Low Power Mode operation. The host power supply voltages including ripple, droop and noise below 100 kHz for VccTxRx and VccMgmt are 3.135 V Minimum, 3.3 V Nominal, and 3.465 V Maximum.

Table 3: Low Power Mode Operation

Parameter	Symbol	Min	Nom	Max	Unit
Power Consumption	P_0	-	-	0.5	W
Instantaneous peak current at hot plug	Icc_ip_0	-	-	80	mA
Sustained peak current at hot plug	Icc_sp_0	-	-	70	mA
Steady state current	Icc_0	-	-	58	mA

4.5.3 Host Board Power Supply Noise Output

For Host Board Power Supply Noise Output see Subclause 5.5.3 in SFF-8679

4.5.4 Module Power Supply Noise Output

For Module Power Supply Noise Output see Subclause 5.5.4 in SFF-8679

4.5.5 Module Power Supply Noise Tolerance

For Module Power Supply Noise Tolerance see Subclause 5.5.5 in SFF-8679

4.6 ESD

The following is an exception to the second paragraph of Subclause 5.6 in SFF-8679. All microQSFP Module and host contacts shall withstand 1 000 V electrostatic discharge based on Human Body Model per JEDEC JESD22-A114-B.

5. Mechanical and Board Definition

5.1 Introduction

The Module defined in this clause is illustrated in Figure 6. All Pluggable Modules and direct attach cables are designed to mate to the Connector and Cage design defined in this specification. Several Cage to bezel options are allowed. Both metal spring finger and elastomeric EMI solutions are permitted. The microQSFP optical interface shall meet one of the Optical Interfaces defined in Subclause 5.10, and shall mate and unmate with the plug on the optical fiber cabling. Latching mechanism pull tabs are not defined and are not shown.

The overall package dimension shall conform to the indicated dimensions and tolerances indicated in clause 5. The mounting features shall be located such that the products are mechanically interchangeable with the Cage and Connector system. In addition, the overall dimensions and mounting requirements for the Cage and Connector system on a circuit board shall be configured such that the products are mechanically, electrically, and thermally interchangeable and the overall dimensions and insertion requirements for the optical Connector and corresponding fiber optic cable plug shall be such that the products are mechanically and optically interchangeable.

Note: All dimensions are in mm.

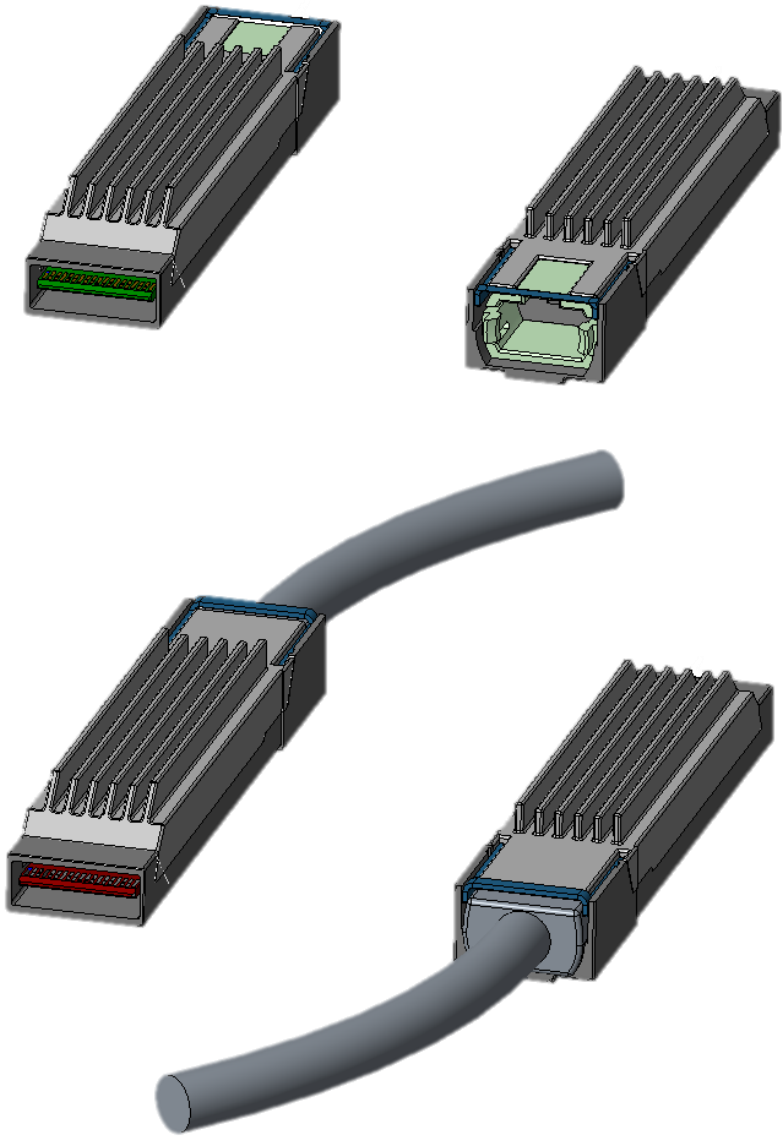

Figure 6 — microQSFP Pluggable Module and Direct Attach Cable Rendering

5.2 microQSFP Reference Datums and Component Alignment

A listing of the reference datums for the various components is contained in Table 4. The alignments of some of the datums are noted. The relationship of the Module, Cage, and Connector relative to the Host Board and Bezel is illustrated in Figure 7 by the location of the key datums of each of the components. In order to reduce the complexity of the drawings, all dimensions are considered centered unless otherwise specified.

Table 4 – Definition of Reference Datums

Datum	Description	Figure Location
A	Bottom surface of Module	Figure 6
B	Latching surface of Module	Figure 6
C	Width of Module	Figure 6
D	Pad surface of Module pc board	Figure 7
E	Front leading surface of Module pc board	Figure 7
F	Width of Module pc board	Figure 7
G	Top surface of host pc board	Figure 8 & 9
H	*Host board thru hole #1 to accept Connector guide post	Figure 8 & 9
J	Host board thru hole #2 to accept Connector guide post	Figure 8 & 9
K	Seating surface of Electrical Connector	Figure 12
L	Rear surface of Electrical Connector	Figure 12
M	Connector slot width	Figure 12
N	*Electrical Connector alignment pin	Figure 12
P	Top Surface of Electrical Connector	Figure 12
R	Seating plane of Cage on host pc board	Figure 13
S	Front surface of Cage	Figure 13
T	Width of inside of Cage	Figure 13
U	**Host board thru hole #1 to accept Cage Pin	Figure 8
V	**Cage Pin #1	Figure 13
* Datums H & N are aligned when assembled (see Figure 7)		
** Datums U & V are aligned when assembled (see Figure 7)		

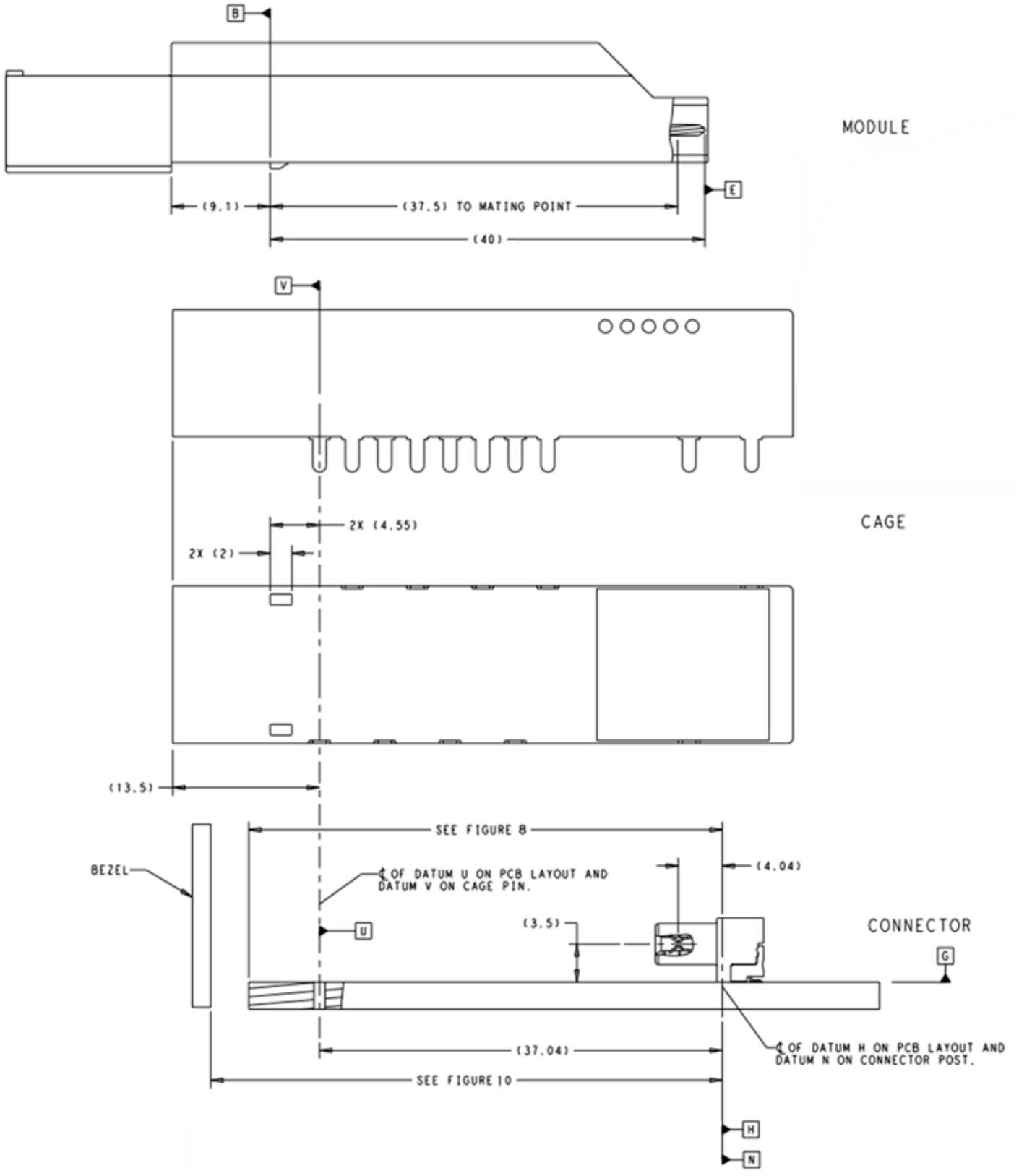

Figure 7 — microQSFP Datum Alignment, Depth

5.3 microQSFP Module Mechanical Package Dimensions

A common mechanical outline is used for all microQSFP Modules and direct attach cables. The Module shall provide a means to self-lock with the Cage upon insertion; means to accomplish self-locking is open to vendor implementation, provided it meets the

dimensions in Figure 8. The package dimensions for the microQSFP Module are defined in Figure 8 and Figure 9.

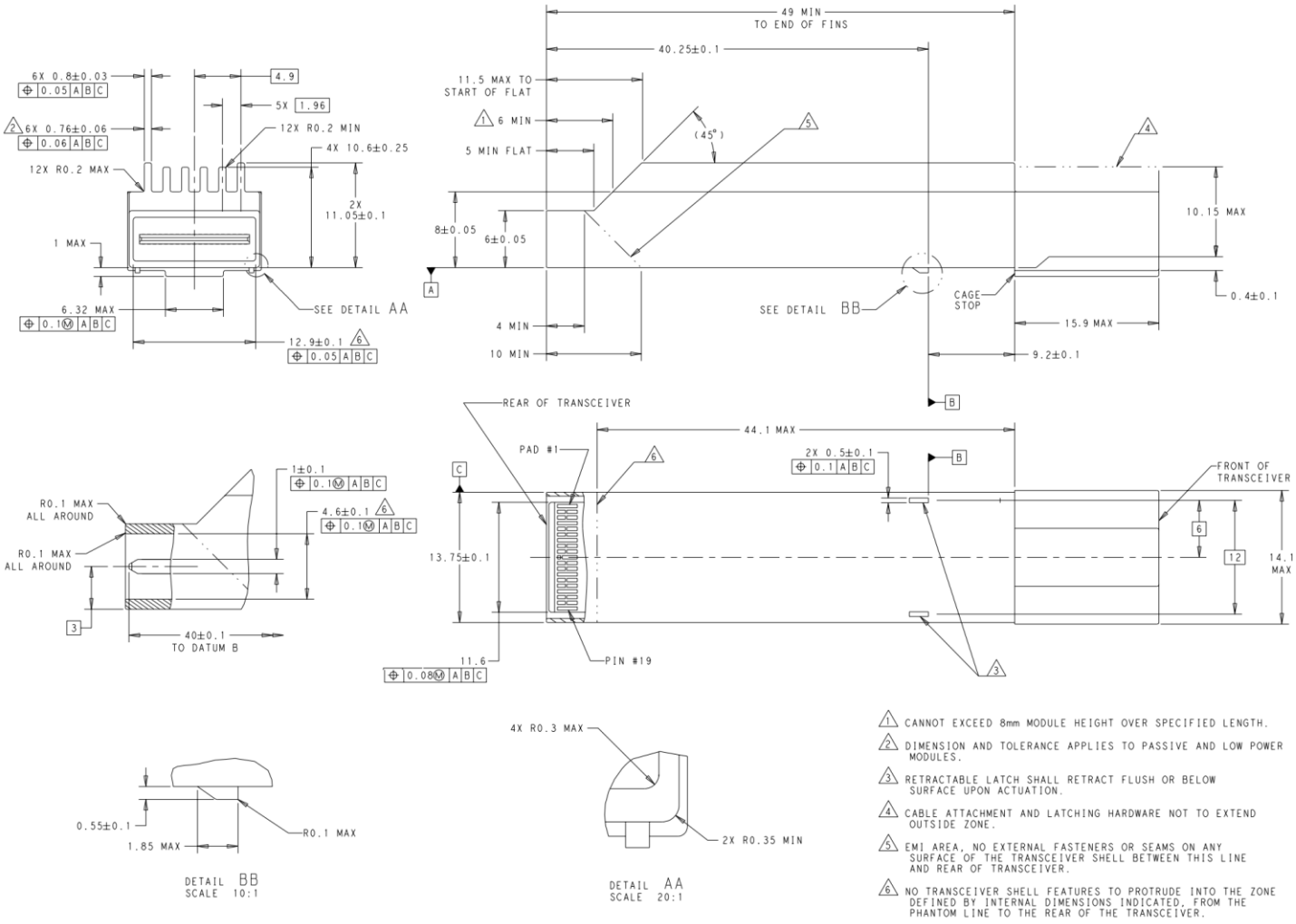

Figure 8 — Drawing of microQSFP Module

5.3.1 Mating of microQSFP Module PCB to microQSFP Electrical Connector

The microQSFP Module contains a printed circuit board that mates with the microQSFP electrical Connector. The pads are designed for a sequenced mating:

First mate – ground contacts
Second mate – power contacts
Third mate – signal contacts

The pattern layout for the microQSFP Printed Circuit Board is shown in Figure 9.

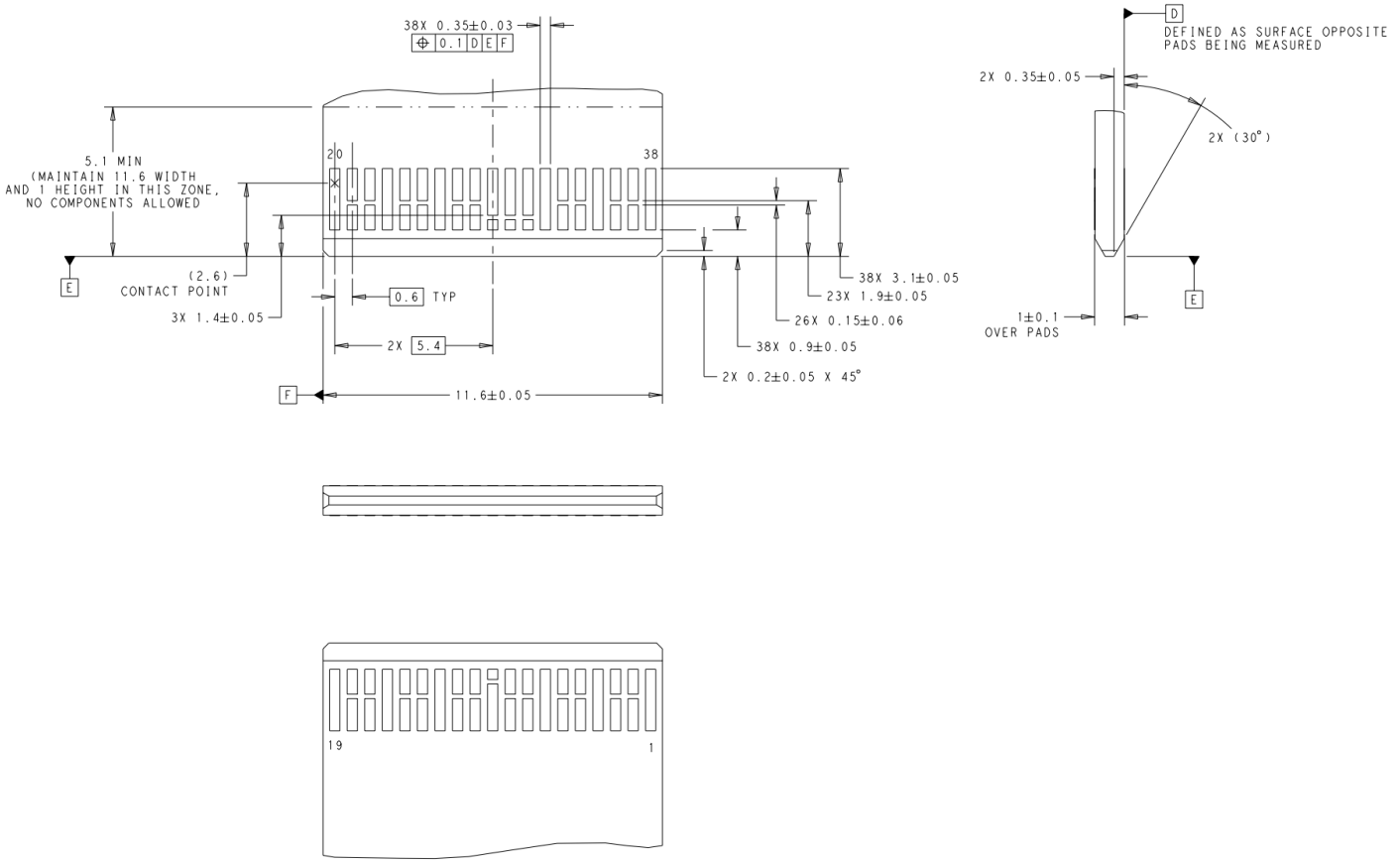

Figure 9 — Pattern Layout for microQSFP Printed Circuit Board

5.4 Host PCB Layout

A typical host board mechanical layout for attaching the microQSFP Connector and Cage System is shown in Figure 10 and Figure 11. Location of the pattern on the host board is application specific. See Subclause 5.6 for details on the location of the pattern relative to the bezel.

To achieve 28Gb/s performance pad dimensions and associated tolerances shall be adhered to and attention paid to the host board layout.

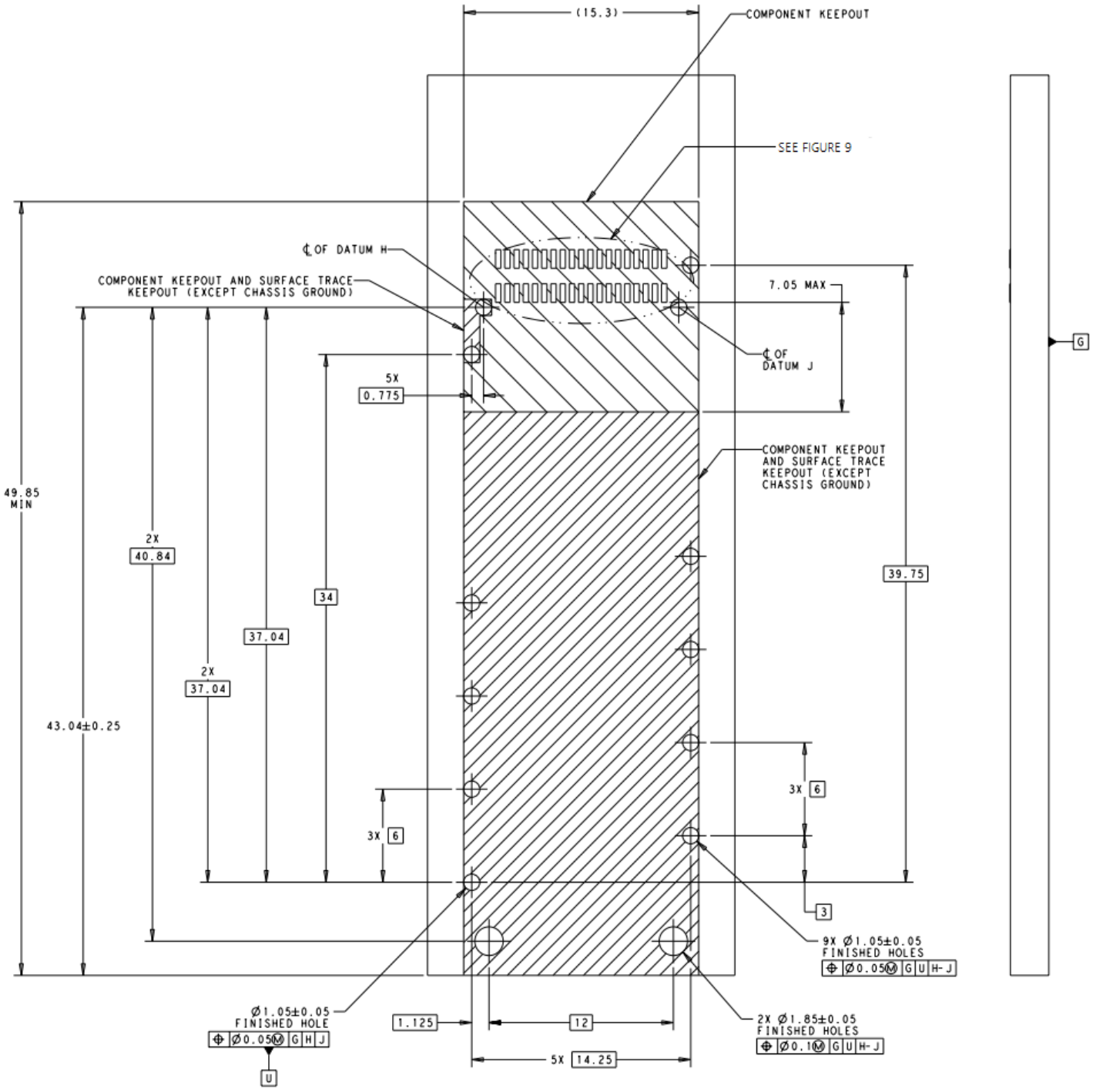

Figure 10 — microQSFP Host PCB Mechanical Layout

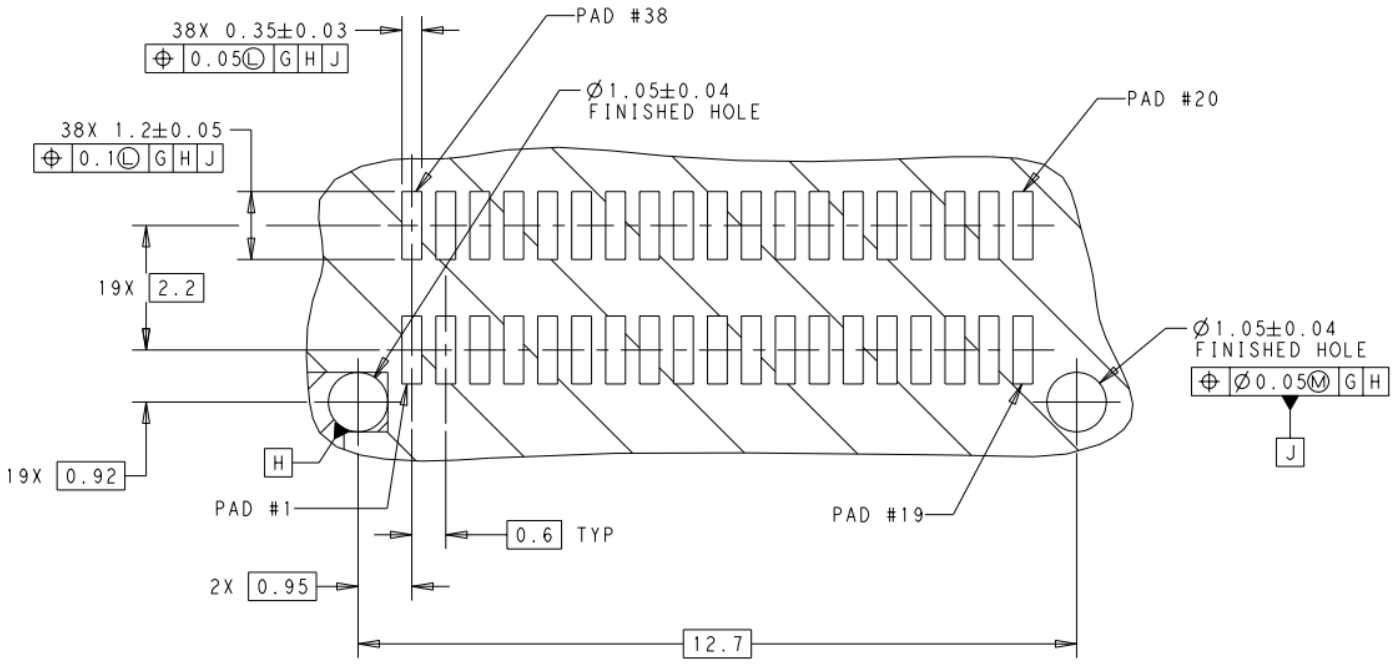

Figure 11 — microQSFP Host PCB Mechanical Layout

5.4.1 Insertion, Extraction and Retention Forces for microQSFP Modules

The requirements for insertion forces, extraction forces and retention forces are specified in Table 5. The microQSFP Cage and Module design combinations shall ensure excessive force applied to a cable does not damage the microQSFP Cage or host Connector. If any part is damaged by excessive force, it should be the cable or media Module and not the Cage or host Connector which is part of the host system. Cable to microQSFP Module retention shall be appropriate to the application, performance can be verified by following industry test methods such as EIA-364-36B or other appropriate specifications.

Table 5 — Insertion, Extraction and Retention Forces

Measurement	Min	Max	Units	Comments
microQSFP Module insertion	0	60	N	Module insertion into host Connector & Cage.
microQSFP Module extraction	0	30	N	Module extraction from host Connector & Cage
microQSFP Module retention with latch engaged	90	N/A	N	No damage to Module below 90N
Cage retention in Host Board	90	N/A	N	Force to be applied in a direction normal to host board top surface, no damage to Cage
Insertion / removal cycles, Connector / Cage	100	N/A	Cyc.	Number of cycles for the Connector and Cage with multiple Modules.
Insertion / removal cycles, microQSFP Module	50	N/A	Cyc.	Number of cycles for an individual Module.

5.5 Color Coding and Labeling of microQSFP Modules

Color coding may be defined by vendor specific requirements or by industry agreements. In the absence of such definition, the colors below may be used.

An exposed feature of the microQSFP Module (a feature or surface extending outside of the bezel) are color coded as follows:

Beige for 850nm
Blue for 1310nm
White for 1550nm

Each microQSFP Module shall be clearly labeled. The complete labeling need not be visible when the microQSFP Module is installed and the bottom of the device is the recommended location for the label. Labeling shall include:

Appropriate manufacturing and part number identification
Appropriate regulatory compliance labeling
A manufacturing traceability code

The label should also include clear specification of the external port characteristics such as:

Optical wavelength
Required fiber characteristics
Operating data rate
Interface standards supported
Link length supported

The labeling shall not interfere with the mechanical, thermal or EMI features.

5.6 Bezel for Systems using microQSFP Modules

Host enclosures that use microQSFP devices should provide appropriate clearances between the microQSFP Modules to allow insertion and extraction without the use of special tools and a bezel enclosure with sufficient mechanical strength. The microQSFP Module insertion slot should be clear of nearby moldings and covers that might block convenient access to the latching mechanisms, the microQSFP Module, or the cables that plug directly into the Cage.

5.6.1 Bezel for the Thru Bezel Cage Assembly

The front surface of the Cage assembly passes through the bezel.

Two EMI solutions may be implemented for the thru bezel Cage. If EMI spring fingers are used, they make contact to the inside of the bezel cutouts. If an EMI gasket is used, it makes contact to the inside surface of the bezel. To accept all Cage designs, both bezel surfaces shall be conductive and connected to chassis ground.

The minimum recommended host board thickness for belly to belly mounting of the Connector and Cage assemblies is 2.2 mm.

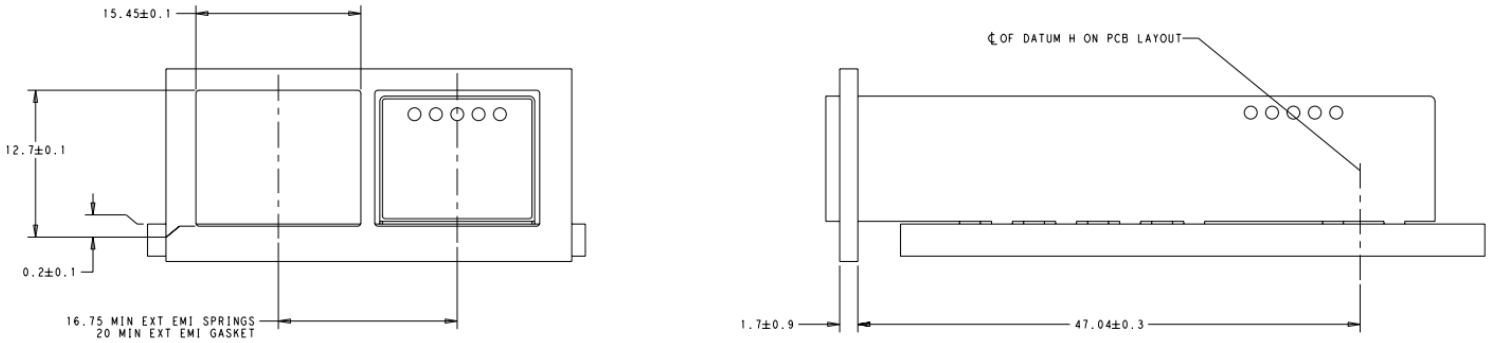

Figure 12 — Recommended Bezel Design for Cages that extend into or thru Bezel

5.7 microQSFP Electrical Connector Mechanical

The microQSFP Connector is a 38-contact, right angle surface mount Connector and is shown in Figure 13. The mechanical specifications for the Connector are listed in Table 5 and shown in Figure 14.

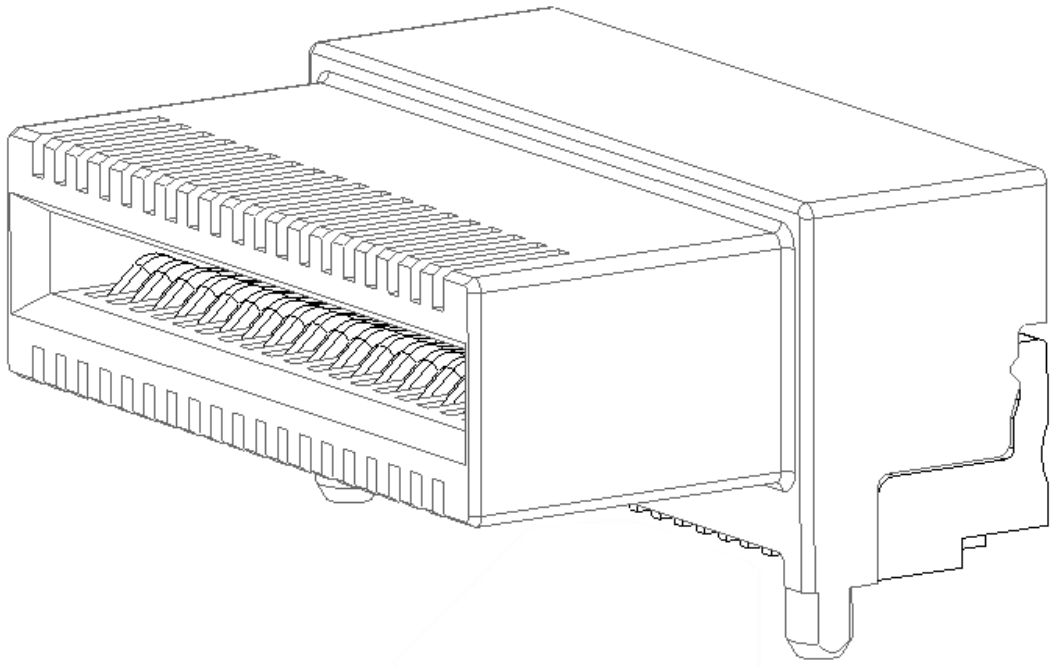

Figure 13 — microQSFP Module Electrical Connector Illustration

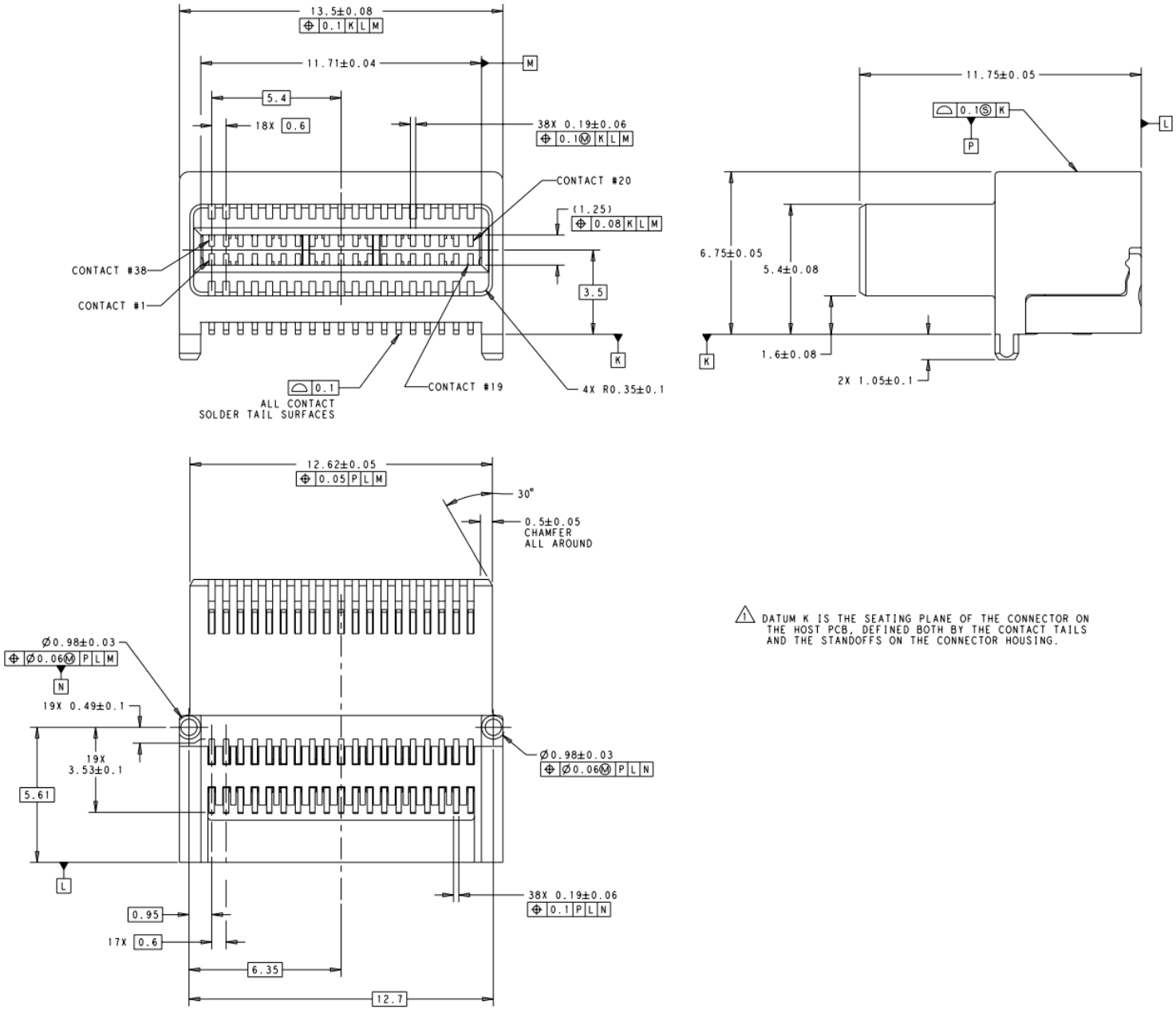

Figure 14 — microQSFP Electrical Connector Specification

5.8 Individual microQSFP Cage Assembly

For microQSFP a Cage Assembly is utilized that passes through the bezel. The detailed drawings for the Cage assembly options are shown in Figure 15. The purpose of the blocking tab is to prevent damage to the Connector should a Module be inserted in an incorrect orientation.

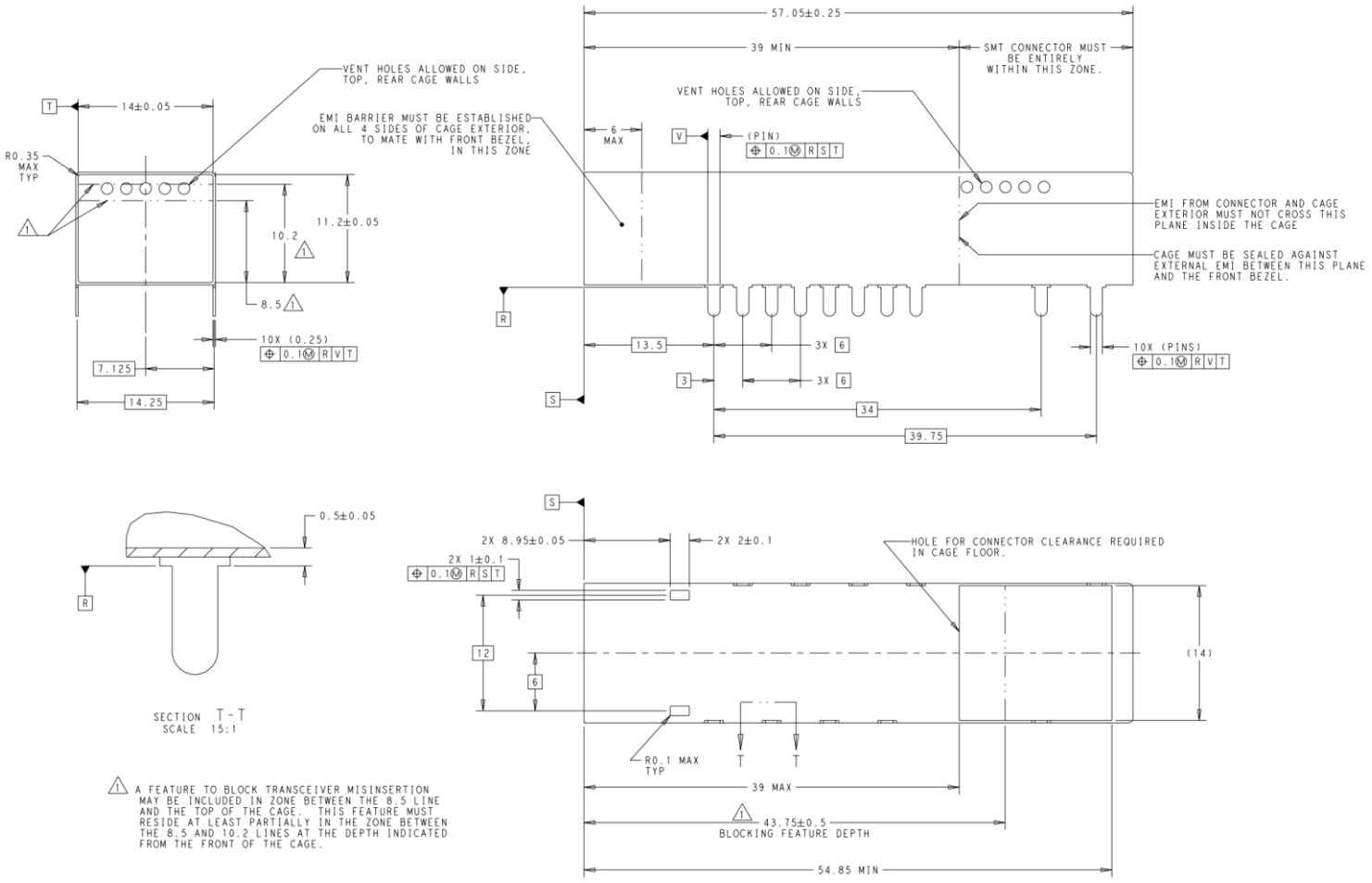

Figure 15 — 1-by-1 Thru Bezel Cage Design

5.9 EMI Cover

In order to prevent contamination of the internal components and to optimize EMI performance, it is recommended that an EMI Cover be inserted into the Cage assembly when no Module is present. The conductivity of the materials should be chosen for the EMI Cover to block EMI emissions. The EMI cover shall be designed such that is can be inserted into a Cage and Connector as defined in this specification.

5.10 Optical Interface

The microQSFP optical interface port shall be either a male MPO connector as specified in IEC 61754-7 (see Figure 16a) or a dual LC as specified in IEC 61754-20 (see Figure 16b).

The four fiber positions on the left as shown in Fig. 14a, with the key slot up, are used for the optical transmit signals (Channel 1 through 4). The fiber positions on the right are used for the optical receive signals (Channel 4 through 1).

The central four fibers may be physically present.
Two alignment pins are present.

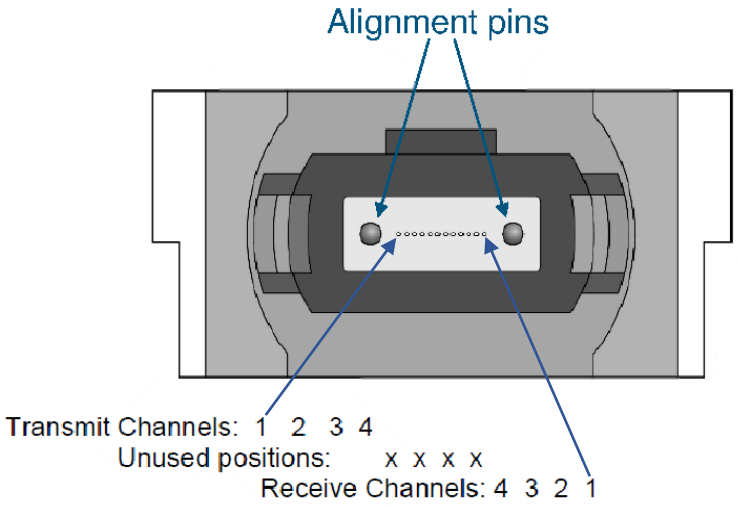

Figure 16a — microQSFP Optical Receptacle and Channel Orientation for MPO Connector (Viewed from Front of Module)

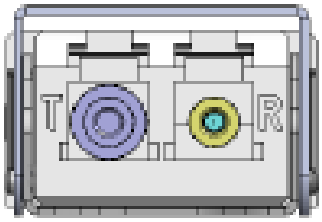

Figure 16b — QSFP+ Optical Receptacle and Channel Orientation for dual LC Connector (Viewed from Front of Module)

5.11 MPO Optical Cable connection

Aligned key (Type B) MPO patchcords should be used to ensure alignment of the signals between the Modules. The aligned key patchcord is defined in TIA-568 and shown in Figure 16c. The optical Connector is orientated such that the keying feature of the MPO receptacle is on the top.

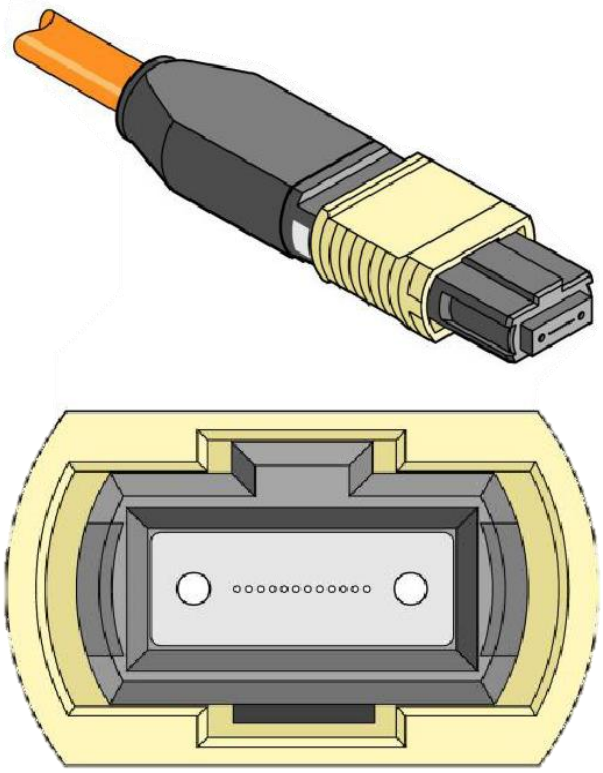

Figure 16c — microQSFP MPO Optical Patchcord

6. Thermal

6.1 Thermal Requirements

The microQSFP Module shall operate within one or more of the case temperatures ranges defined in Table 6. The temperature ranges are applicable between 60m below sea level and 1800m above sea level, (Ref. NEBS GR-63) utilizing the host systems designed airflow. Case temperature measurement location shall be vendor specific similar to the current situation with SFP, QSFP, etc. form factors.

Table 6 Temperature Range Class of operation

Class	Case Temperature Range
Standard	0 through 70C
Extended	-5 through 85C
Industrial	-40 through 85C

microQSFP is designed to allow for up to 24 adjacent Modules in a single row, ganged, and/or belly-to-belly, with the appropriate thermal design for cooling / airflow (Ref. NEBS GR-63). Airflow around the module and through the Cage is not filtered by design nor is it a requirement of this specification.

6.2 Thermal Management Considerations

For microQSFP cooling is typically achieved by allowing front to back airflow to pass through the Module. Ambient air outside the chassis is intended to enter the chassis around the microQSFP Module and through Cage instead of only through other openings in the chassis bezel. This ambient air shall pass around cooling features of the Module, pass into the Cage assembly, and then exit the Cage assembly into the chassis. This design intent allows for increased port density within a chassis rack, while allowing ambient air to not only cool the Module but also allow that air to pass through into the chassis to cool components deeper inside the chassis.

Additionally, the microQSFP Cage should have ventilation holes as allowed in Figure 15. The dimensions of these vent holes are determined by the Cage manufacturers within the bounds set forth in Figure 15. Care should be taken to ensure adequate ventilation through the Cage is attained and that EMI is prevented from penetrating the Cage.

7. Management Interface

7.1 Introduction

A management interface, as defined in SFF-8636, is specified in order to enable flexible use of the Module by the user.

7.2 microQSFP Memory Map

This microQSFP Specification adopts the management interface and memory map requirements found in Clauses 4, 5, and 6 of SFF-8636 except as noted here in Clause 7. This exception list was generated from SFF-8636 rev 2.7. Fields previously used in SFF-8636 Rev 2.7 that are no longer used are now reserved in microQSFP.

Table 7 microQSFP Exceptions to SFF-8636 Memory Map Definition

Location	Disposition	Register Name	Description
Lower Memory Byte 0 & Byte 128	Identifier value for microQSFP added to SFF-8024 Table 4-1	Identifier	Additional module type for microQSFP Identifier Value 17h.
Lower Memory Byte 2 bits[7:4]	Changed from Reserved to Current Module state, see Table 9 for encoding.	Module_State	Current module state, encoded (see Table 9 for encoding.)
Lower Memory Byte 2 bit 0	Change from Data_Not_Ready flag to Reserved	Data_Not_Ready flag	Functionality replaced by State_changed flag, this register bit is reserved for future use.
Lower Memory Byte 6 bit 0	Change from Initialization Complete flag to State_changed flag	State_changed flag	Flag to indicate state transition from a transient state to a parked state. Setting this flag shall result in the module asserting IntL. This flag shall be cleared upon read.
Lower Memory Byte 93 bit 0	Change from Power override to Reserved	Power override	microQSFP does not have a dedicated LPMODE contact, this register bit is reserved for future use
Lower Memory Byte 93 bit 1	Change Power Set Description	Power_Set	Power set to Low Power Mode Default 1
Lower Memory Byte 93 bit 2	Change from High Power Class Enable to Reserved	High Power Class Enable	This bit is no longer needed, because the host can read all power classes and determine support, so clearing the Power set bit will enable power classes 1-7. This register bit is reserved for future use.

Lower Memory Byte 103 bit 0	Changed from Reserved to M-Module State Change	M-Module State Change	Masking Bit for Module State Change Flag.
Lower Memory Byte 129 bits [7:5]	Change power classes for bits [7:6], change bit 5 from Reserved to power class use.	Extended Identifier Values	microQSFP needs additional power classes not designated in SFF-8636. See Table 8 for encodings.
Lower Memory Byte 129 bits [1:0]	Change from Unused and Power Classes to Reserved.	Extended Identifier Values	These bits are no longer needed to define power classes, all power classes are defined in bits [7:5]. See Table 8 for encodings.
Lower Memory Byte 114 bits [3:0]	Changed from Reserved to Max_DataPathInit_Duration	Max_DataPathInit_Duration	Max duration of DataPathInit state. See Table 10 for encodings.
Lower Memory Byte 114 bits [7:4]	Changed from Reserved to Max_TX_TurnOn_Duration	Max_TX_TurnOn_Duration	Max duration of TX_TurnOn state. See Table 10 for encodings.

The reader should also note that microQSFP adds a VccMgmt supply that does not exist in SFF-8636. Therefore, all references to Vcc in SFF-8636 are applicable to the VccTxRx rail and not the VccMgmt rail.

7.2.1 Extended Identifier

The extended identifier provides additional information about the free side device. For example, the identifier indicates if the free side device contains a CDR function and identifies the power consumption class it belongs to.

The power class identifiers specify maximum power consumption over operating conditions and lifetime with all supported settings set to worst case values.

Table 8 Extended Identifier Values (Lower Memory Byte 129 bits 7:0)

Bit	Device Type
7,6,5	000: Power Class 1 (0.5 W max.)
	001: Power Class 2 (1.5 W max.)
	010: Power Class 3 (2.5 W max.)
	011: Power Class 4 (3.5 W max.)
	100: Power Class 5 (5.0 W max.)
	101: Power Class 6 (7.0 W max.)
	110: Power Class 7 (9.0 W max.)
	111: Power Class 8 (>9.0 W) *
4	0: No CLEI code present in Page 02h
	1: CLEI code present in Page 02h
3	0: No CDR in TX
	1: CDR Present in TX
2	0: No CDR in RX
	1: CDR Present in RX
1-0	Reserved
* See vendor documentation for specific power requirements.	

7.2.2 Module_State Register Encodings

Encodings for the Module_State register are shown in Table 9. Passive copper cables implemented with static EEPROMs shall utilize encoding 0000b.

Table 9 Module_State Encodings (Lower Memory Byte 2 bits 7:4)

Encoding Bit order (7,6,5,4)	State
0000b	Module does not support state machine
0001b	MgmtInit
0010b	Configure
0011b	DataPathInit
0100b	TX_Off
0101b	TX_TurnOn
0110b	MissionMode
0111b	RevertLowPwr
1000b-1111b	Reserved

7.2.3 Transient State Duration Encodings

The Max_DataPathInit_Duration (Lower Memory Byte 114 bits 3:0) and Max_TX_TurnOn_Duration (Lower Memory Byte 114 bits 7:4) registers are used to allow the module to inform the host of the maximum duration of transient states. Note that the module may interrupt the host at any time before the maximum duration reported, to report that the state is complete. Table 10 defines the encodings used for both registers.

Table 10 Transient State Duration Encodings (Lower Memory Byte 114 bits 7:4 & bits 3:0)

Encoding Bit order (7,6,5,4) & (3,2,1,0)	Maximum State Duration
0000b	Maximum state duration is less than 1 ms. This state is not reported in the Module_State register, and no interrupt is generated upon entry into next parked state
0001b	1 ms <= maximum state duration < 5 ms
0010b	5 ms <= maximum state duration < 10 ms
0011b	10 ms <= maximum state duration < 50 ms
0100b	50 ms <= maximum state duration < 100 ms
0101b	100 ms <= maximum state duration < 500 ms
0110b	500 ms <= maximum state duration < 1 s
0111b	1 s <= maximum state duration < 5 s
1000b	5 s <= maximum state duration < 10 s
1001b	10 s <= maximum state duration < 1 min
1010b	1 min <= maximum state duration < 5 min
1011b	5 min <= maximum state duration < 10 min
1100b	10 min <= maximum state duration < 50 min
1101b	Maximum state duration >= 50 min
1110b	Reserved
1111b	Reserved

7.3 microQSFP State Machine

The module behaviors and available interfaces to the host are defined using the state machines shown in Figure 17 and Figure 18 below. The Figure 17 state machine is applicable to modules that contain active electronics in the high-speed data path. The Figure 18 state machine is applicable to passive copper cable assemblies.

States with dashed boxes are transient states with a variable duration, depending on the module implementation. The module reports the maximum duration of the DataPathInit and TX_TurnOn states in the Max_DataPathInit_Duration and Max_TX_TurnOn_Duration registers in the memory map. In general, host interactions with the module should be minimized during these transient states, with memory map accesses limited to read-only static register content. Dynamic register content is unreliable during transient states.

States with solid boxes are parked states, which require host interaction. The duration of these states is completely controlled by the host, with exit from the state only occurring after the module receives the applicable trigger from the host. The trigger for each state is defined in the state diagrams and detailed descriptions below.

The memory map contains a Module_State register to report the current state of the module. Some transient states may be so short that the Module_State register is not updated. Refer to Subclause 7.2.2 for the definition of the Module_State register encodings and Subclause 7.2.3 for transient state duration encodings.

All modules shall power up in Low Power Mode upon insertion or assertion or deassertion of ResetL. When active modules are in low power mode, the module receiver high speed signal outputs shall be quiescent and the transmitter optical outputs shall be disabled. All passive copper cable assemblies shall be fully functional immediately upon insertion.

When the host software has configured the active module and is ready to activate the high-speed data path, the host software shall put the module into High Power Mode, using the control bits in Lower Memory Page Byte 93 control bits 0 and 1.

In Table 5-4 of Subclause 5.5.2 of SFF-8679, the default value for the Power_Set bit is 1. Both bits 1 and 0 shall be set to move the module to High Power Mode.

The host shall apply power to both the VccMgmt and VccTxRx rails upon module insertion.

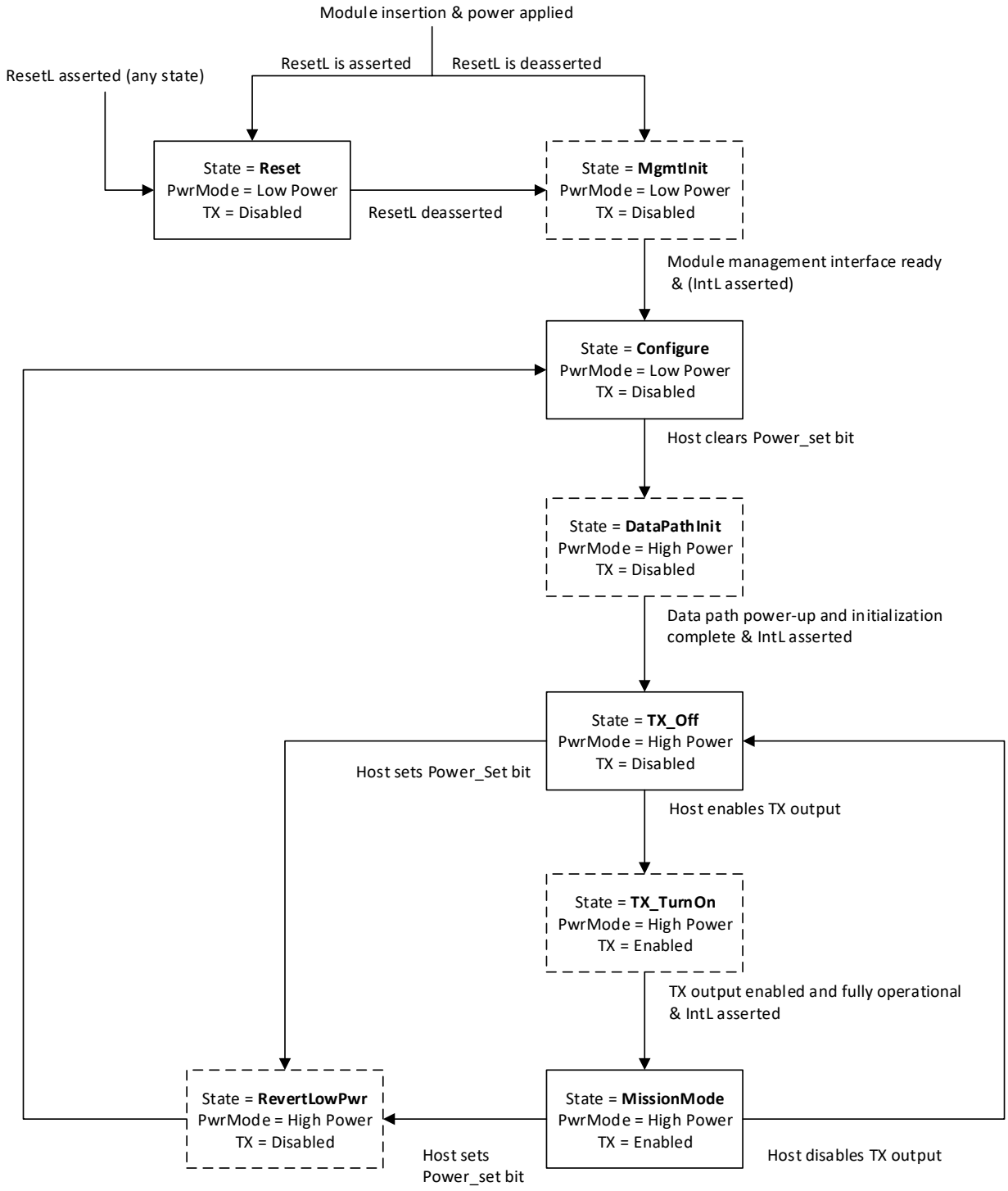

Figure 17 – microQSFP Active Module State Machine

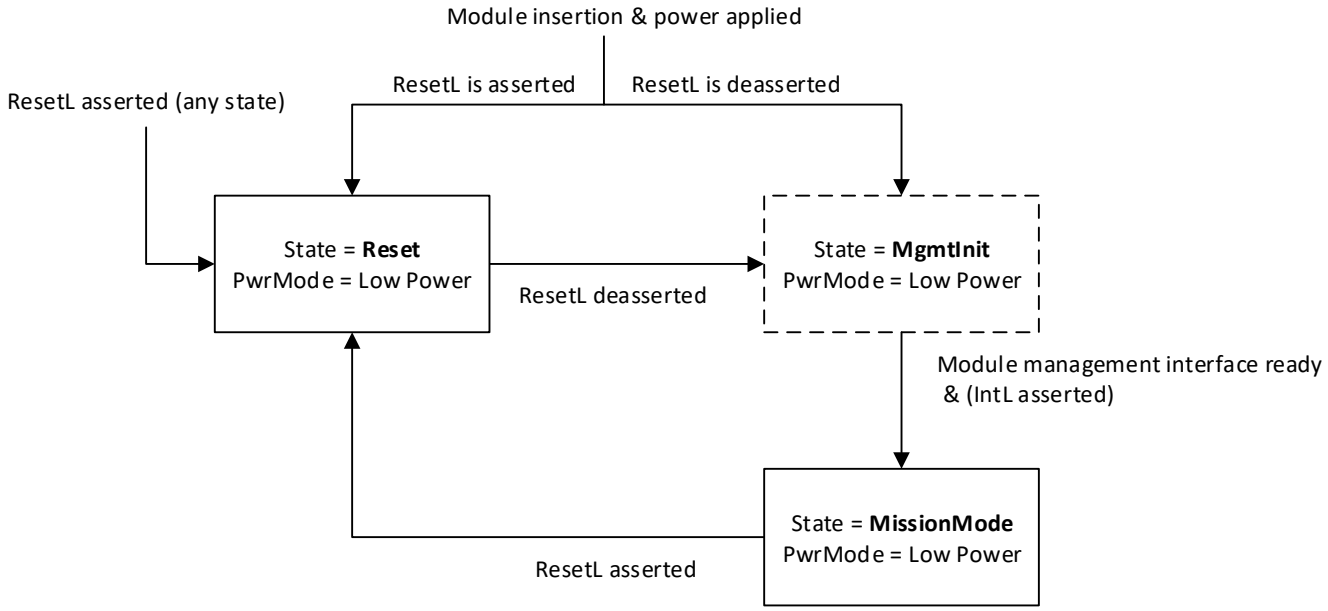

Figure 18 – microQSFP Passive Copper Cable State Machine

7.3.1 MgmtInit State (Transient)

The MgmtInit state is a transient state that is entered any time the module is brought out of Reset, due to deassertion of the ResetL signal or upon initial insertion and application of power to the VccMgmt and VccTxRx contacts. For implementations supporting only passive copper cables, the host may or may not apply VccTxRx. The MgmtInit state is applicable to both active modules and passive copper cable assemblies.

During this state, the module shall initialize the management interface and configure the memory map for access by the host. The module may perform limited power-up of the high-speed data path circuitry, however the module shall remain in Low Power mode throughout this state. The module may ignore all 2-wire serial interface transactions while in this state.

The module shall not assert IntL during MgmtInit. If catastrophic faults occur, the module shall transition immediately to the Configure state to report the fault. The module shall report all non-catastrophic faults and warnings that are valid after transitioning to the Configure state.

Before the module exits this state, all memory map register locations shall be set to their power-on defaults. The module shall have completed MgmtInit in accordance with Mgmtinit_Duration as defined in Table 12. The duration of the MgmtInit state, MgmtInit_Duration, is the time from power on (defined as the instant when supply voltages reach and remain at or above the minimum level specified in SFF-8679 Table 5-6), hot plug or rising edge of reset until the module has configured the memory map to default conditions and activated the management interface.

7.3.2 Configure State (Parked)

The Configure state is a parked state only applicable to active microQSFP modules. During this state, the host may configure the module using the management interface and memory map. Some example configuration activities include reading the ID and device property fields, setting CDR and other channel attributes and configuration of monitor masks. Details of host-module interactions in the Configure State are implementation dependent and are outside the scope of this specification.

Upon entry into the Configure state, the module shall set the Module_State register to the Configure state, set the State_Changed flag and any applicable fault and warning flags that are valid after transitioning to the Configure state, and assert the IntL

signal. The host shall read the State_Changed flag along with all other fault and warning flags to deassert the IntL signal.

Throughout the Configure state, the module shall remain in Low Power Mode and the TX output shall be disabled. The module shall ignore host requests to enable the module TX while in this state.

Prior to exit from this state, the host shall enable all applicable host transmitters and provide compliant signals, so that the module can configure TX electrical input circuitry while in the DataPathInit state.

When the host has completed module configuration, the host may enable full power up of the module by writing a 0 in the Power_Set bit (Lower Memory Page Byte 93 bit 1) in the memory map.

7.3.3 DataPathInit State (Transient)

The DataPathInit state is a transient state where the module powers up the TX and RX high speed data path electronics and applies module configuration settings defined in the module memory map. This state is applicable only to active modules. Example activities during this state include adaptation of module CTLE, TX CDR lock, and RX equalization enable, etc. The duration of the DataPathInit state, DataPathInit_Duration, is the time from the falling clock edge after the Stop bit of the Power_Set bit write transaction to the assertion of the initialization completed IntL (IntL Vout = Vol), both times are observed at the module. The maximum duration of the DataPathInit state shall be identified by the module vendor in the Max_DataPathInit_Duration register, Lower Memory Byte 114 bits [3:0]. Encodings for Max_DataPathInit_Duration are defined in Table 10.

Upon entry into the DataPathInit state, the module shall enter High Power mode and set the Module_State register to the DataPathInit state.

Throughout the DataPathInit state, the TX output shall be disabled. The module shall ignore host requests to enable the module TX while in this state. The host shall minimize 2-wire serial transactions while in this state. Dynamic memory map content may be unreliable while in this state and should not be read or written.

The module shall not assert IntL during DataPathInit. If catastrophic faults occur, the module shall transition immediately to the TX_Off state to report the fault. The module shall report all non-catastrophic faults and warnings that are valid after transitioning to the Tx_Off state.

When the module has completed power-up and initialization of the TX and RX high-speed data path circuitry, the module shall transition to the TX_Off state.

7.3.4 TX_Off State (Parked)

The TX_Off state is a holding state where the module TX and RX electronics has been fully powered and configured but is waiting for the host to enable the module TX output. This state is only applicable to active modules.

Upon entry into the TX_Off state, the module shall set the Module_State register to the TX_Off state, set the State_Changed flag and any valid fault and warning flags, and assert the IntL signal. The host shall read the State_Changed flag along with all other fault and warning flags to deassert the IntL signal.

Throughout the TX_Off state, the module shall remain in High Power Mode and the TX output shall be disabled.

A Host enables the transition to the TX_TurnOn state TX by writing a 0 in each and every TX Disable bit (Lower Memory Byte 86 bits 3:0).

7.3.5 TX_TurnOn State (Transient)

The TX_TurnOn state is a transient state where the module enables its TX output. This state is applicable only to active modules. The duration of the TX_TurnOn state, TX_TurnOn_Duration, is the time from the falling clock edge after the Stop bit of the last TX Disable bit write transaction to until the optical output rises above 90% of nominal, both times are observed at the module. The maximum duration of the TX_TurnOn state shall be identified by the module vendor in the Max_TX_TurnOn_Duration register, Lower Memory Byte 114 bits [7:4]. Encodings for Max_TX_TurnOn_Duration are defined in Table 10.

Upon entry into the TX_TurnOn state, the module shall set the Module_State register to the TX_TurnOn state.

The host shall minimize 2-wire serial transactions while in this state. Dynamic memory map content may be unreliable while in this state and should not be read or written.

For modules whose TX output turn-on time is less than 1 ms, the TX_TurnOn state shall be bypassed by the module, with no assertion of the IntL signal.

The module shall not assert IntL during TX_TurnOn. If catastrophic faults occur, the module shall transition immediately to the MissionMode state to report the fault. For warnings and non-catastrophic faults, the module shall report all valid faults and warnings only after transitioning to MissionMode.

When the module TX output is fully operational, the module shall transition to the MissionMode state.

7.3.6 MissionMode State (Parked)

The module is fully operational while in the MissionMode state. The MissionMode state is applicable to both active and passive modules.

Upon entry into the MissionMode state, the module shall set the Module_State register to the MissionMode state, set the State_Changed flag and any valid fault and warning flags. The host shall read the State_Changed flag along with all other fault and warning flags to deassert the IntL signal.

For active modules, the module shall be in High Power Mode throughout the MissionMode State. Host TX outputs shall be enabled and fully operational in this state. Host requests to disable the TX output shall result in disablement of TX outputs and a transition to the TX_Off state. The module transitions to the RevertLowPower state when the host writes a 1 in the Power_Set bit (Lower Memory Byte 93 bit 1).

For passive modules, the module shall remain in Low Power Mode throughout the MissionMode State.

7.3.7 RevertLowPower State (Transient)

The RevertLowPower state is a transient state where the module power returns to the Low Power Mode. This state is applicable only to active modules.

Upon entry into the RevertLowPower state, the module shall set the Module_State register to the RevertLowPower state, disable the TX output, and set the TX Disabled bits in the memory map. The TX output shall remain disabled throughout the RevertLowPower state.

The host shall minimize 2-wire serial transactions while in this state. Dynamic memory map content may be unreliable while in this state and should not be read or written.

The module shall remain in the RevertLowPower state until the module is in Low Power Mode. Any faults or warnings that occur during the RevertLowPower state shall be ignored. When the module reached a power level consistent with Low Power Mode, the module shall transition to the Configure state.

7.3.8 Reset State (Parked)

The Reset state can be entered from any state by assertion of the ResetL signal. Module behavior when ResetL is asserted is defined in SFF-8679 5.2.2. Deviations from and clarifications to SFF-8679 are defined as follows. For passive copper cables, holding the EEPROM in reset is optional. The TX output for active modules shall be disabled throughout the Reset state. Management interface transactions initiated by the host during the Reset state may be ignored by the module. The Reset state can only be exited by deassertion of the ResetL signal. Upon exit from the Reset state, the module shall enter the MgmtInit state.

7.3.9 Interrupt Flag Applicability Per State

Some module interrupt flags are generated by the state machine, but the majority of the flags are triggered by other sources. The host may choose to mask any flag by setting the appropriate mask bits during the Configure state. Flags that are masked by set mask bits do not generate IntL assertion in all states.

Table 11 shows the interrupts that are available in each state. All interrupts not listed shall be inhibited by the module in the applicable state.

Table 11 Available Interrupts Per State

State	Interrupts available	
Reset	None	
MgmtInit	None	
Configure	State_Changed	
DataPathInit	All interrupts shall be held until transition to TX_Off	
TX_Off	All	
TX_TurnOn	All interrupts shall be held until transition to MissionMode	
MissionMode	All	
RevertLowPwr	None	

7.3.10 Timing Requirements

The following are exceptions and additions to Subclause 8.1 of SFF-8679.

Table 12 Timing Requirements

Parameter	Symbol	Max	Unit	Conditions
Management Initialization Time	MgmtInit	2000	ms	The time from power on (defined as the instant when supply voltages reach and remain at or above the minimum level specified in SFF-8679 Table 5-6), hot plug or rising edge of reset until the module has configured the memory map to default conditions and activated the management interface.
Data Path Initialization Time	DataPathInit	See 7.3.3	-	The time from the falling clock edge after the Stop bit of the Power_Set bit write transaction to the assertion of the initialization completed IntL (IntL Vout = Vol), both times are observed at the module.
TX Turn On Time	TX_TurnOn	See 7.3.5	-	The time from the falling clock edge after the Stop bit of the last TX Disable bit write transaction to until the optical output rises above 90% of nominal, both times are observed at the module.

8. Appendix A

8.1 Introduction

This appendix provides alternate signal symbols and contact numbering to allow the microQSFP form factor to be used for applications that support a PCIe protocol. Two different contact numbering diagrams are described for separate PCIe applications. These alternative applications are not electrically interoperable with the primary contact assignment in Section 4 of this document, however if accidentally interoperated, no damage to the equipment will occur. The alternative assignments in this appendix affect only the power and low speed signals and not the high speed signals. Two styles are described in this appendix, a Type A which can accommodate both active plugs and passive plugs and a Type B which only works with passive plugs that have additional wires dedicated for passing clock signals in addition to the high speed data lines.

This appendix is not intended to modify or supersede the current revision of the PCI Express External Cabling Specification. It is intended to be aligned with the forthcoming PCI Express External Cable Specification Rev 3 which is being finalized at the time this appendix was being written. The method for determining which type of module is plugged in is beyond the scope of this appendix.

8.2 Type A Electrical Specification for PCIe Applications

The Type A electrical interface for PCIe applications defines the contact numbering that allows microQSFP to be used for PCI Express External Cabling Specification applications that supports both active modules and passive modules.

8.2.1 Type A Electrical Interface for PCIe applications

Figure 19 shows the signal symbols and contact numbering for a Type A microQSFP Module edge Connector for PCIe applications. The diagram shows the Module PCB edge as a top and bottom view. There are 38 contacts intended for high speed signals, low speed signals, power, and ground connections.

The module contains a printed circuit board that mates with the electrical connector. The pads are designed for a sequenced mating:

First mate - ground contacts
Second mate - power contacts
Third mate - signal contacts

For EMI protection the signals to the connector should be shut off when the module is removed. Standard board layout practices such as connections to Vcc and GND with Vias, use of short and equal-length differential signal lines, use of microstrip-lines and 50 Ohm terminations are recommended. The chassis ground (case common) of the module should be isolated from the module's circuit ground, GND, to provide the equipment designer flexibility regarding connections between external electromagnetic interference shields and circuit ground, GND, of the module.

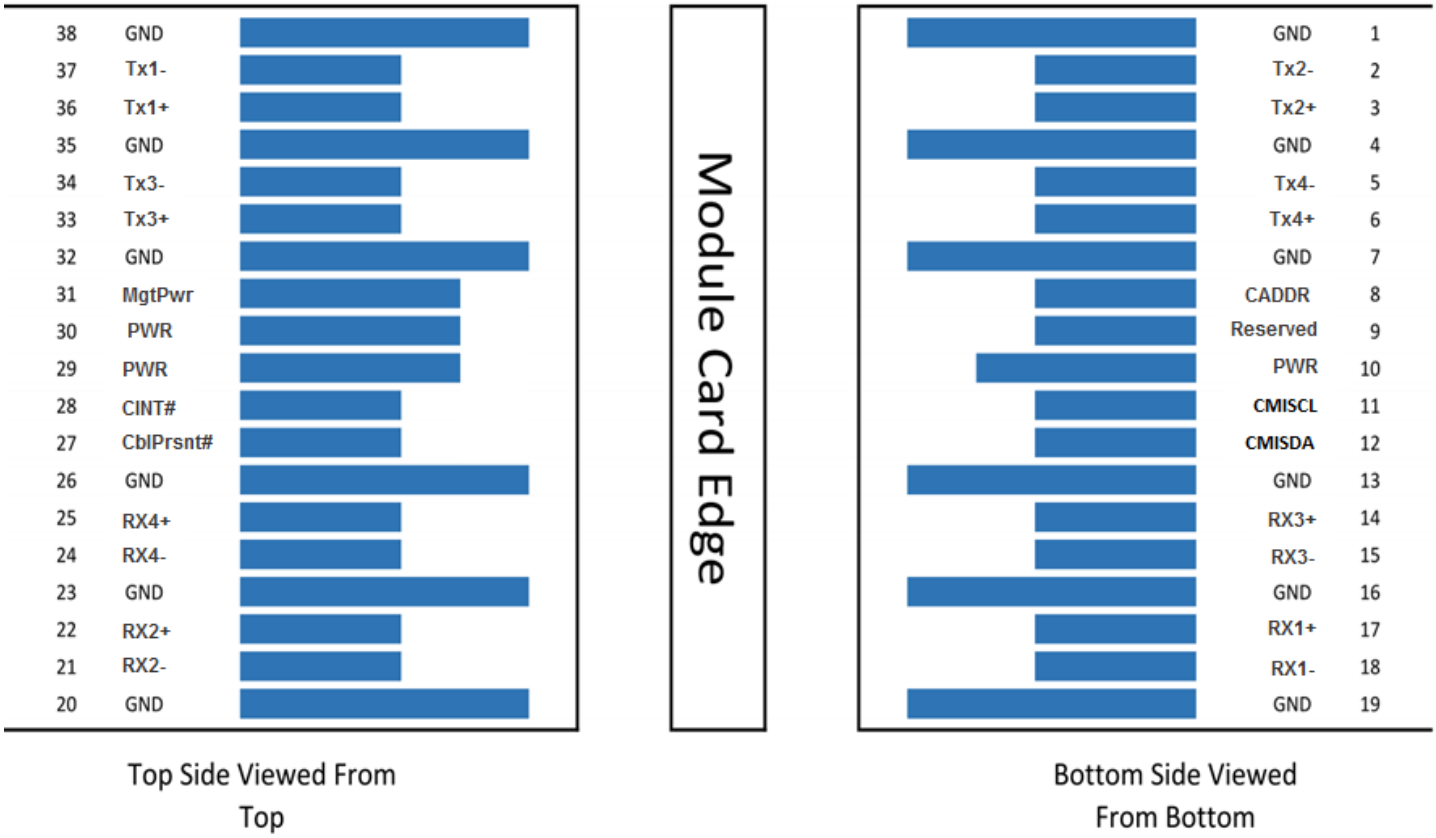

Figure 19 microQSFP Module Pad Layout for PCIe Type A

Table 13: microQSFP Module Electrical Interface Map

#	Logic	Symbol	Name	Plug Sequence	Notes
1		GND	Signal Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Signal Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Signal Ground	1	1
8	LVTTL-I	CADDR	Cable Management Device Address	3	
9	LVTTL-I	Reserved	Not Used, Leave Open	3	
10		PWR	+3.3V Power Supply for high-speed data path ICs	2	2
11	LVCMOS-I/O	CMISCL	Management Interface Clock Line	3	
12	LVCMOS-I/O	CMISDA	Management Interface Data Line	3	
13		GND	Signal Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Signal Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Signal Ground	1	1
20		GND	Signal Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Signal Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Signal Ground	1	1
27	LVTTL-O	CblPrsnt#	Cable Present Detect	3	
28	LVTTL-O	CINT#	Interrupt	3	
29		PWR	+3.3V Power Supply for high-speed data path ICs	2	2
30		PWR	+3.3V Power Supply for high-speed data path ICs	2	2
31		MGTPWR	Management Interface Power Supply	2	2
32		GND	Signal Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Signal Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Signal Ground	1	1

Note 1: GND is the symbol for signal and supply (power) common for the microQSFP Module. All are common within the microQSFP Module and all Module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
Note 2: Each Vcc contact is limited to maximum of 1 A. The Host shall apply power to all Vcc contacts (PWR and MGTPWR) concurrently. All PWR contacts may lead to a common 3.3 V Power Supply in the module. This 3.3 V Power Supply shall be electrically isolated from the MGTPWR Power Supply in the module.

Figure 20 shows an example block diagram of the connectivity between the host PCB and the Type A active microQSFP module.

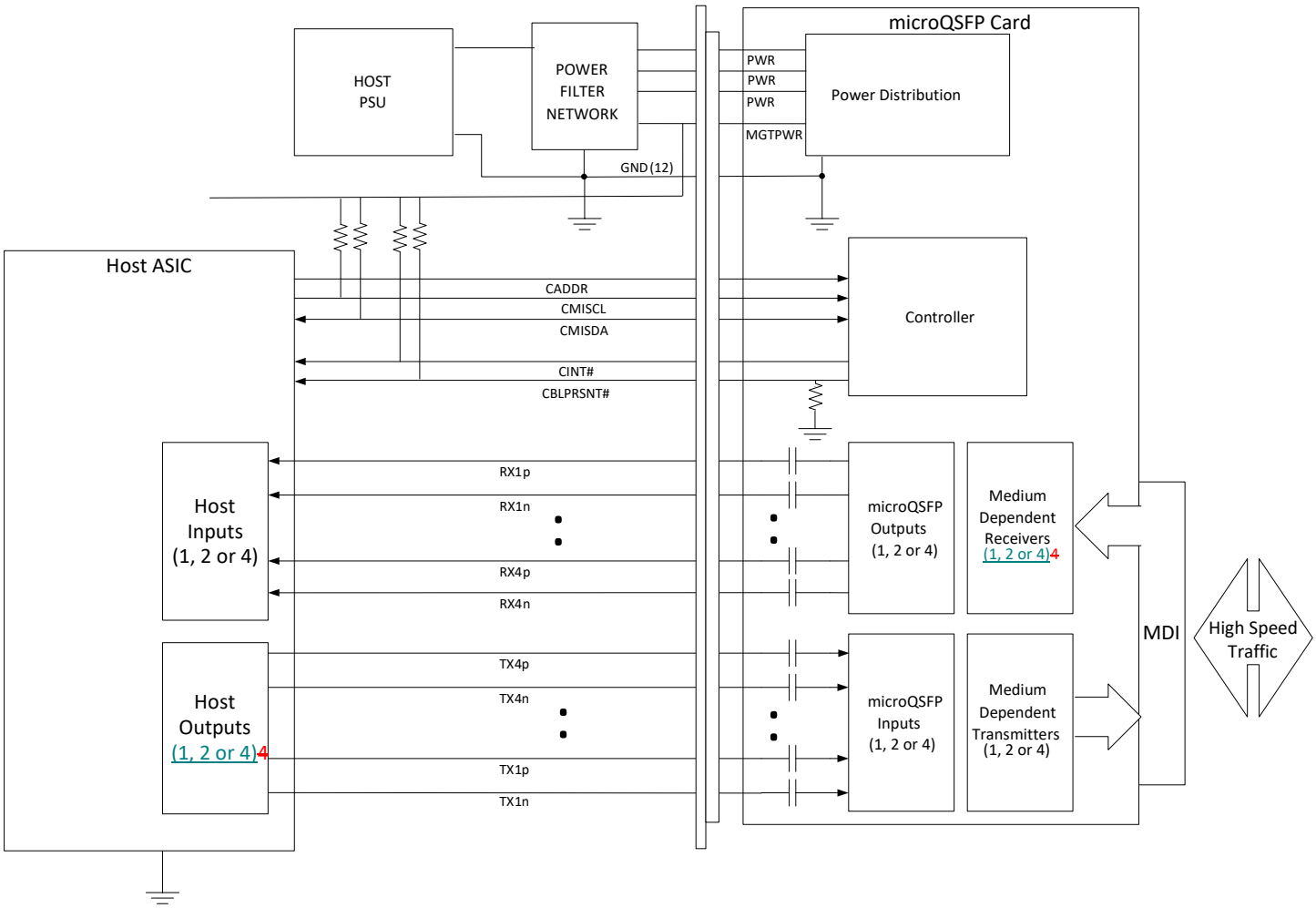

Figure 20a: Example microQSFP Host Board and Optical Module Block Diagram for PCIe Type A

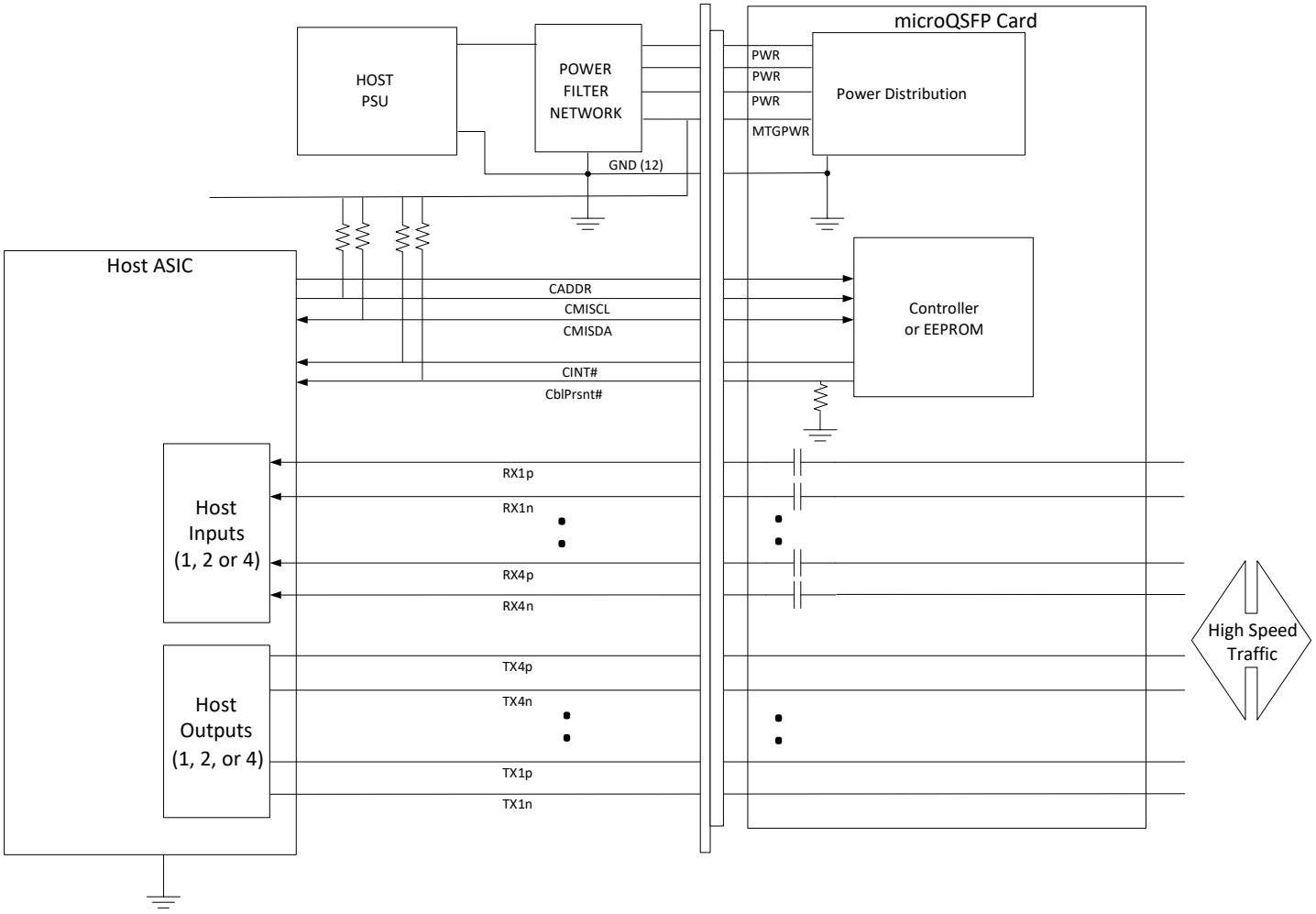

Figure 20b Example microQSFP Host Board and Copper Cable Module Block Diagram for PCIe Type A

8.3 Type B Electrical Interface for PCIe Applications

Type B electrical interface for PCIe applications defines the contact numbering that allows microQSFP to be used for PCI Express External Cabling Specification applications that only support passive copper cables. Type B electrical interface passes low speed out-of-band signals through extra wires in the cable assembly.

Figure 21 shows the signal symbols and contact numbering for the Type B microQSFP Module edge Connector for PCIe applications. The diagram shows the Module PCB edge as a top and bottom view. There are 38 contacts intended for high speed signals, low speed signals, power, and ground connections.

The module contains a printed circuit board that mates with the electrical connector. The pads are designed for a sequenced mating:

First mate - ground contacts
Second mate - power contacts
Third mate - signal contacts

For EMI protection the signals to the connector should be shut off when the module is removed. Standard board layout practices such as connections to Vcc and GND with Vias, use of short and equal-length differential signal lines, use of microstrip-lines and 50 Ohm terminations are recommended. The chassis ground (case common) of the module should

be isolated from the module's circuit ground, GND, to provide the equipment designer flexibility regarding connections between external electromagnetic interference shields and circuit ground, GND, of the module.

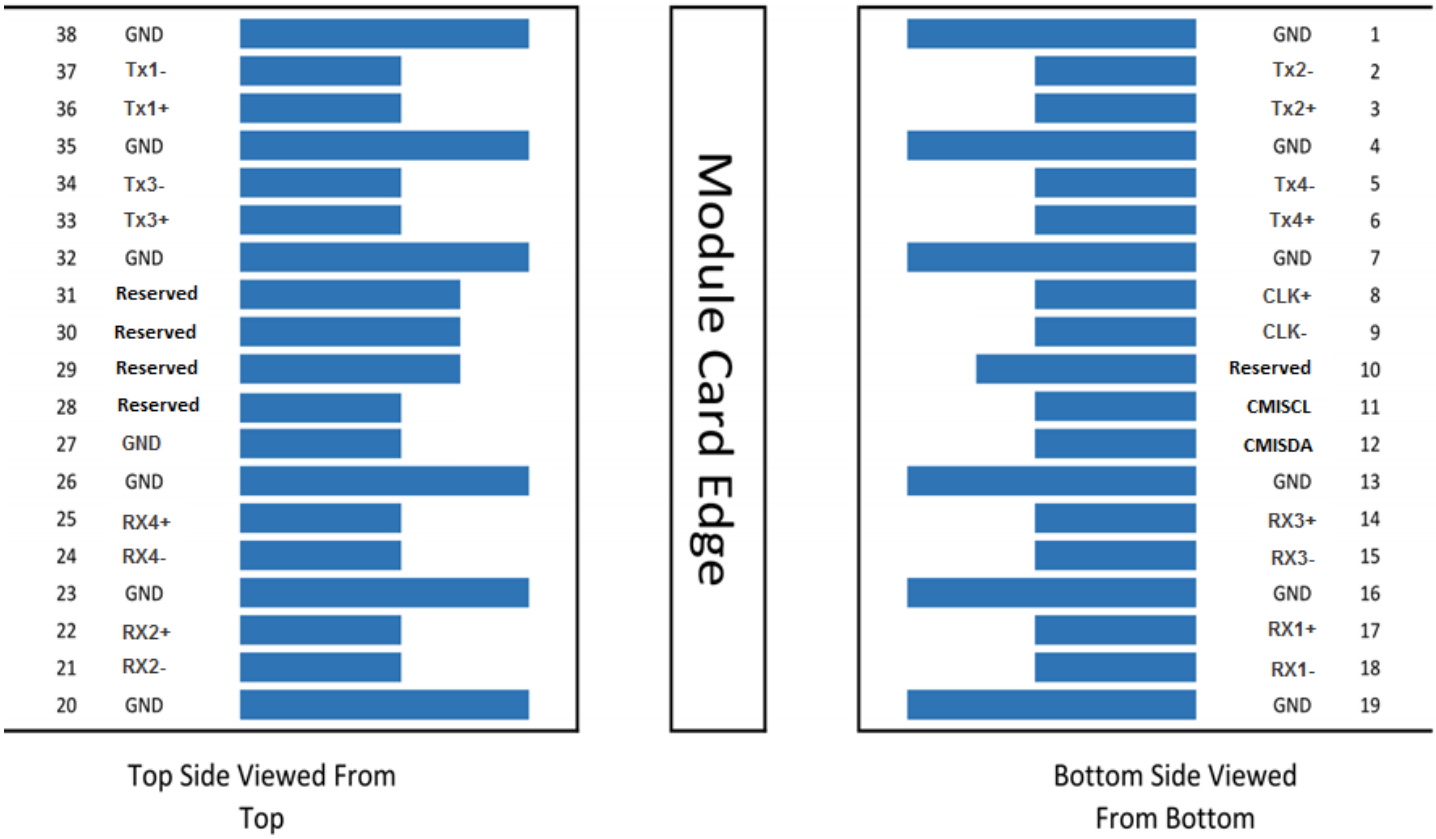

Figure 21 microQSFP Module Pad Layout for PCIe Type B

Table 14: microQSFP Module Electrical Interface Map

#	Logic	Symbol	Name	Plug Sequence	Notes
1		GND	Signal Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Signal Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Signal Ground	1	1
8	CML-I/O	CLK+	Low Speed Clock Signal Non-Inverted	3	
9	CML-I/O	CLK-	Low Speed Clock Signal Inverted	3	
10		Reserved	Not Used, Leave Open	2	
11	LVCMOS-I/O	CMISCL	Management Interface Clock Line	3	
12	LVCMOS-I/O	CMISDA	Management Interface Data Line	3	
13		GND	Signal Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Signal Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Signal Ground	1	1
20		GND	Signal Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Signal Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Signal Ground	1	1
27	LVTTL-O	GND	Signal Ground	3	1
28	LVTTL-O	Reserved	Not Used, Leave Open	3	
29		Reserved	Not Used, Leave Open	2	
30		Reserved	Not Used, Leave Open	2	
31		Reserved	Not Used, Leave Open	2	
32		GND	Signal Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Signal Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Signal Ground	1	1

Note 1: GND is the symbol for signal and supply (power) common for the microQSFP Module. All are common within the microQSFP Module and all Module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Figure 22 shows an example block diagram of the connectivity between the Type B host PCB and the Type B microQSFP module for copper cable implementations.

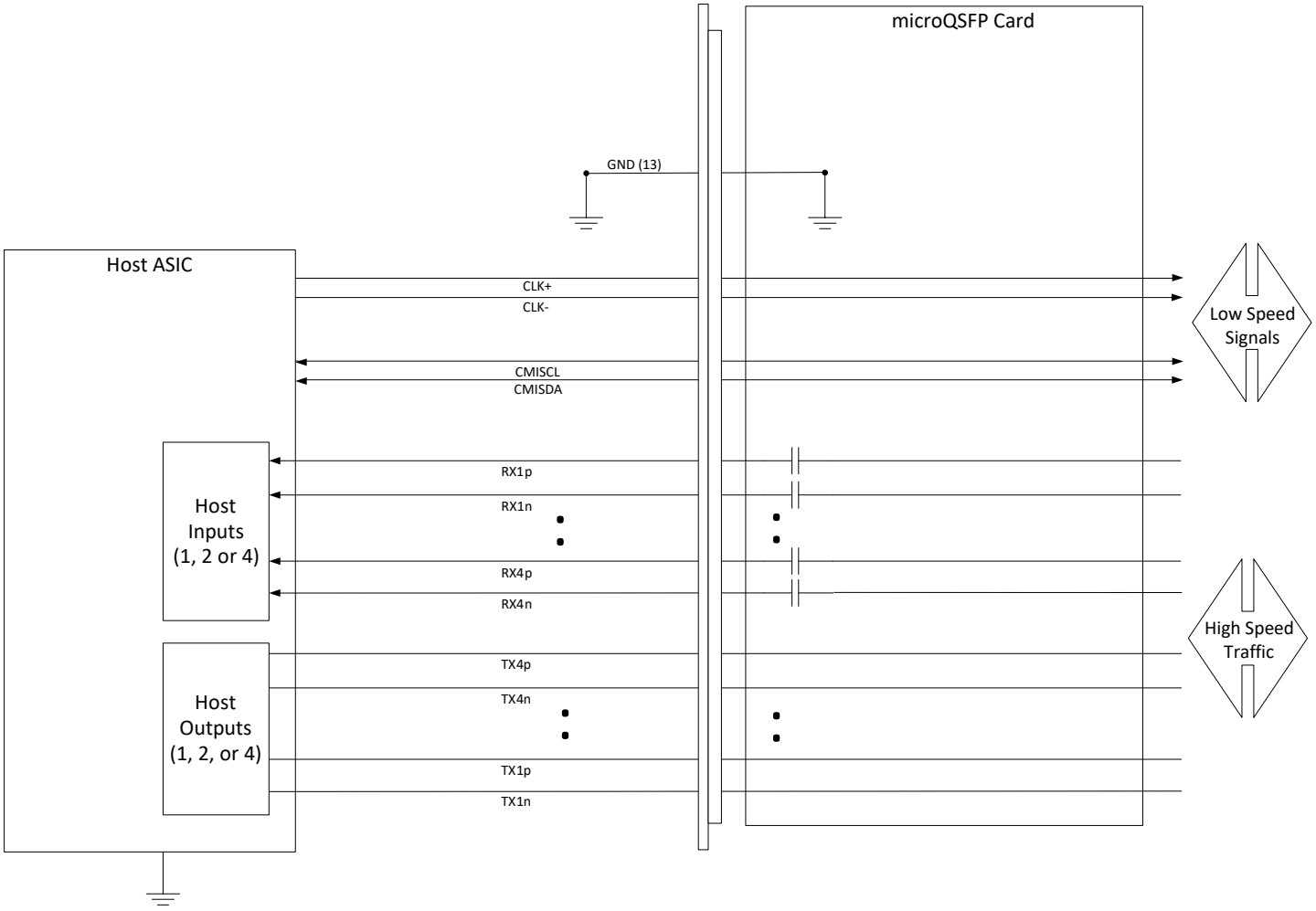

Figure 22 Example microQSFP Host Board and Copper Cable Module Block Diagram for PCIe Type B

9. Appendix B

9.1 1, 2, and 4 Channels Examples

microQSFP is a high density pluggable form factor that can be used in 1, 2 and 4 channel versions. These can be used in both point to point and breakout applications as shown in the Figure 23 image. Being a four-channel form factor, microQSFP can be used to support many applications. The following list as well as the configurations shown in figure 23 are provided solely as examples of some of the use cases and are not intended to be a comprehensive summary.

1, 2 or 4 times 10GE
1, 2 or 4 times 25GE
1 or 2 times 50G (25G Ethernet Consortium)
1, 2 or 4 times 50GE (803.2cd draft)
1 times 100GE (802.3-2015)
1 or 2 times 100GE (802.3cd draft)
1 times 200GE (802.3cd draft)

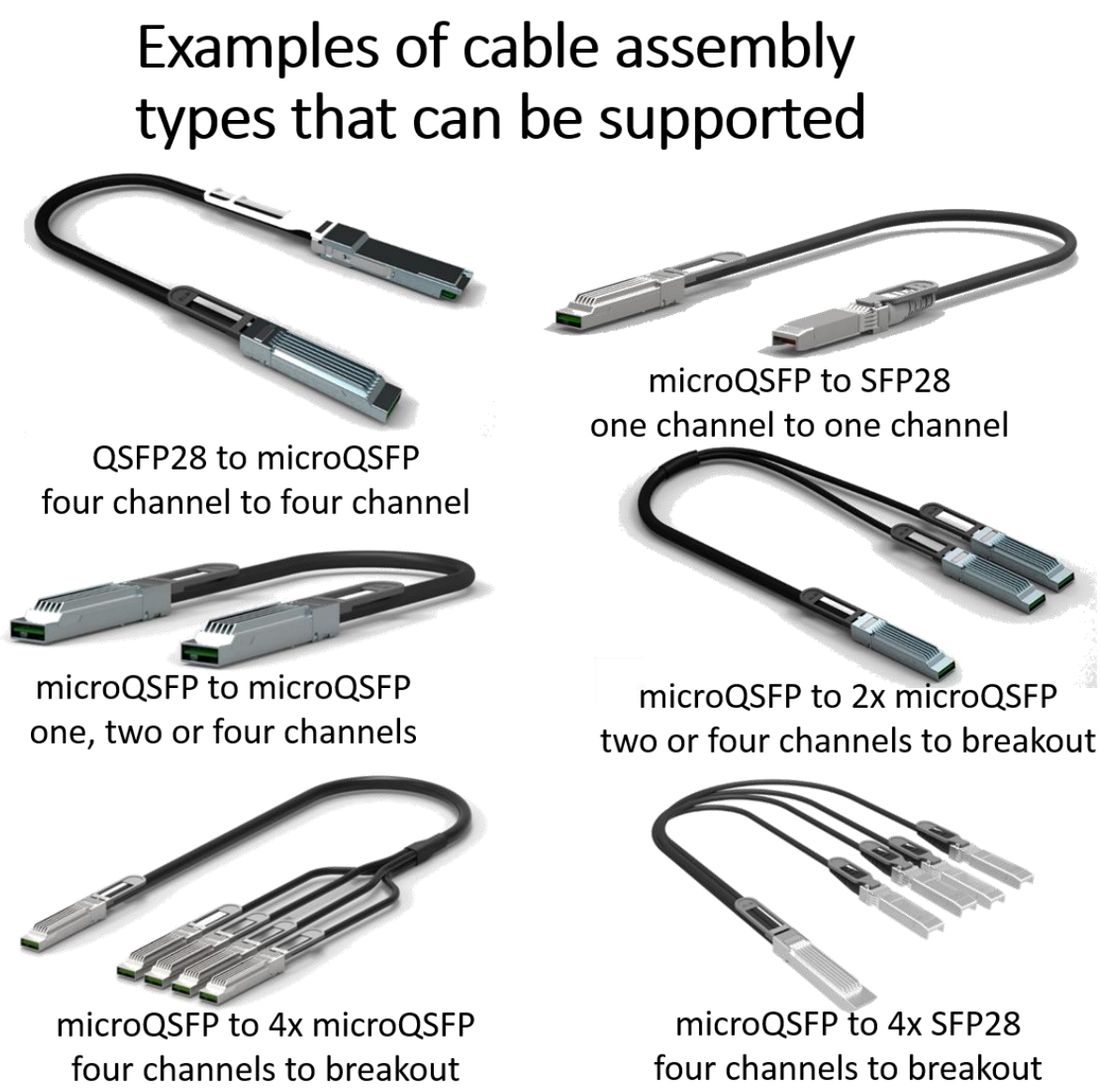

Figure 23 Example Cable Module Assemblies

In all cases where 1 or 2 channels are supported, these could possibly be either depopulated (unused channels) or 'breakout' applications.

There are two key requirements to make sure that microQSFP works in x1, x2 and x4 applications; 1) using the correct electrical contacts as defined in clause 4.1.1, and 2) correct coding of the module management interface per SFF-8636, "Table 6-15, Free side Device properties (page 00H Bytes 108-114)". Note that this portion of SFF-8636 is also included in this microQSFP specification Clause 7 and is repeated here only for clarity. These fields identify the channel usage of both the near end and the far end of the link.