GIGALIGHT 100GBASE-LR4 CFP2 10km Optical Receiver
P/N: GF2R-S101-LR4C

Features

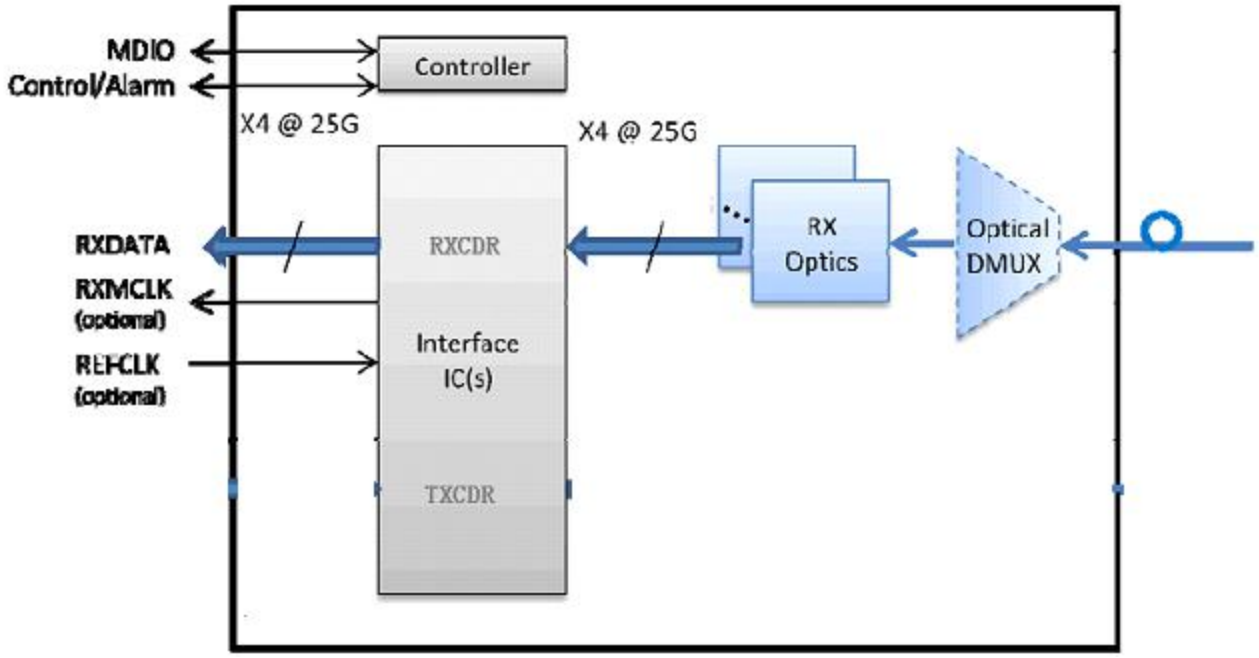
- Operating optical data rate up to 112Gbps
- PIN ROSA only (without Transmitter)
- CFP2 MSA compliant
- Compliant to IEEE 802.3baspecification for 100GBASE-LR4
- Compliant to OTU4
- Transmission distance up to 10km
- Operating electrical serial data rate up to 27.952493Gbps
- 4 parallel electrical serial interface and AC coupling of CML signals
- MDIO real-time digital diagnostic(Optional) and control capabilities
- RX output CDR retiming
- Hot pluggable
- Total Power Consumption<3W
- Operating case temperature 0°C to +70°C
- 3.3V power supply
- Duplex LC receptacle optical interface
- RoHS 6 compliant(lead free)
- Compliant with CFP2 MSA hardware specification
- Compliant with CFP MSA management specification

Applications

- 100GbE IEEE 802.3ba 100GBASE-LR4
- OTN-OTU4
- Switch to switch interface or Switch to router interface

Description

The Gigalight CFP2 100GEBASE-LR4 optical Receiver is a hot pluggable 100Gbps small-form-factor transceiver module .It is compliant with IEEE802.3ba and CFP MSA. The module is a multi-rate optical transceiver and intended to support Telecom and Datacom applications.



100GE CFP2 LR4 single receiver Module Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	Unit	Min	Max
Supply Voltage	VCC3	V	-0.5	3.6
Storage Temperature	Ts	°C	-40	85
Operating Case Temperature	Tc	°C	0	70
Relative Humidity (Non condensation)	-	%	5	95

Recommended Operating Conditions

Parameter	Symbol	Unit	Min	Typ	Max
Operating Case Temperature	Tc	°C	0	-	70
Supply Voltage	VCC	V	3.13	3.3	3.47
Supply Current	ICC	A	-	-	0.9
Power Dissipation	-	W	-	-	3

Optical Characteristics

(Tested under recommended operating conditions, unless otherwise noted)

Parameter	Symbol	Unit	Value		
			Min	Typ	Max
Optical Receiver Characteristics					
Receiver Sensitivity in OMA for Each Lane(100GbE)	SOMA	dBm	-	-	-8.6
Receiver Sensitivity for Each Lane(OTU4)					-10.8
Los Assert		dBm			-12
Los De-assert		dBm	-19		
Los Hysteresis		dBm		1	

Electrical Characteristics

(Tested under recommended operating conditions, unless otherwise noted)

Parameter	Symbol	Unit	Min	Typ	Max	Note
Receiver						
Differential Data Output Swing	Vout,pp	mV	400	-	800	
Differential Signal Output Resistance		Ω	80	-	120	
Differential Signal Input Resistance		Ω	80	-	120	
LOS Fault	-	V	V_{dd3}-0.5	-	V_{dd3}	
LOS Normal	-	V	0	-	+ 0.5	1
Note1: Vdd3 is host +3.3V power supply.						

Low Speed Electrical Interface

Parameter	Symbol	Unit	Min	Max	Note
Input High Voltage	V_{IH}	V	2.0	V_{cc3} + 0.3	
	V_{IL}	V	-0.3	0.8	
Input Low Voltage	V_{OH}	V	V_{dd3}-0.5	V_{dd3} + 0.3	1
	V_{OL}	V	0.0	0.4	
Input Leakage Current	V_{IH}	V	Vdd3*0.7	Vdd3 + 0.5	1
	V_{IL}	V	-0.3	Vdd3*0.3	
Output High Voltage (IOH = 100uA)	V_{OH}	V	Vdd3-0.5	Vdd3 + 0.3	
	V_{OL}	V	0.0	0.4	
Output low Voltage (IOH = 100uA)	IL	uA	-10	10	

Minimum Pulse Width of Control Pin Signal		KHz		400	
1.2V LVCMOS Electrical Characteristics					
Input High Voltage	1.2VIH	V	0.84	1.5	
Input Low Voltage	1.2VIL	V	-0.3	0.36	
Input Leakage Current	1.2IIN	uA	-100	+ 100	
Output High Voltage	1.2V0H	V	1.0	1.5	
Output Low Voltage	1.2V0L	V	-0.3	0.2	
Output High Current	1.2I0H	mA		-4	
Output Low Current	1.2I0L	mA	+4		
Input Capacitance	Ci	pF		10	

Hardware Control Pins

The CFP2 Module support real-time control functions via hardware pins, listed in the following table:

Hardware Control Pins

Pin#	Symbol	Description	I/O	Logic	H	L	Pull-up/down
17	PRG_CNTL1	Programmable Control 1 MSA Default:TRXIC_RSTn , TX&RX ICs reset, “0”:reset;”1”	I	3.3V LVCMOS	per CFP MSA Management Interface Specification		Pull-Up Note1
18	PRG_CNTL2	Programmable Control 2 MSA Default : Hardware Interlock LSB	I	3.3V LVCMOS			Pull-Up Note1
19	PRG_CNTL3	Programmable Control 3 MSA Default:Hardware Interlock MSB	I	3.3V LVCMOS			Pull-Up Note1
26	M0D_L0PWR	Module Low Power Mode	I	3.3V LVCMOS	Low Power	Enable	Pull-Up Note1
28	M0D_RSTn	Module Reset(Invert)	I	3.3V LVCMOS	Enable	Reset	Pull-Down Note2
24	TX_DIS	Transmitter Disable	I	3.3V LVCMOS	Disable	Enable	Pull-Up Note1

Note1: Pull-Up resistor (4.7KOhm to 10 KOhm) is located within the CFP2 module Note2: PuH-Down resistor (4.7KOhm to 10 kOhm) is located within the CFP2 module

Hardware Alarm Pins

The CFP Module supports alarm hardware pins listed in the following table: Hardware Alarm Pins

Pin#	Symbol	Description	I/O	Logic	H	L	Pull-up/down
20	PRG_ALRM1	Programmable Alarm 1 MSA Default:HIPWR_0N	O	3.3V LVCMOS			
21	PRG_ALRM3	Programmable Alarm 3 MSA Default: MOD_FAULT	O	3.3V LVCMOS			
22	MOD_ABS	Module Absent	O	3.3V LVCMOS			
27	RX_LOS	Receiver Loss of Signal	O	3.3V LVCMOS	Absent	Present	Pull-Down Note1
25	PRG_ALRM3	Receiver Loss of Signal	O	3.3V LVCMOS	Loss of Signal	OK	

Note1: Pull-Down resistor (<100ohm) is located within the CFP module. Pull-up should be located on the host

Management Interface Pins(MDIO)

The CFP Module supports alarm, control and monitor functions via an MDIO bus. The CFP MDIO pins are listed in

Pin#	Symbol	Description	I/O	Logic	H	L	Pull-up/down
29	GLB_ALRMn	Global Alarm	I	3.3V LVCMOS	Ok	Alarm	
32	MDIO	Management Data Input Output Bi-Directional Data	I/0	1.2V LVCMOS			
31	MDC	MDIO Clock	I	1.2V LVCMOS			
33	PRTADR0	MDIO Physical Port address bit0	I	1.2V LVCMOS	per MDIO document[5]		
34	PRTADR1	MDIO Physical Port address bit1	I	1.2V LVCMOS			
35	PRTADR2	MDIO Physical Port address bit2	I	1.2V LVCMOS			

Hardware Signaling Pin Timing Requirements

Timing Parameters for CFP2 hardware Signal Pins are listed in the following table.

Parameter	Symbol	Min	Max	Unit	Notes&Conditions
Hardware MOD_LOPWR assert	t_MOD_LOPWR_assert		1	ms	Application Specific May depend on current state Condition when signal is applied .See Vendor Datasheet

Hardware MOD_LOPWR deassert	t_MOD_LOPWR_deassert			ms	Value is dependent upon module start-up time.Please See register〃Maximum High-Power-up ime〃in “CFP MSA Management Interface Specification”
Receiver Loss of Signal Assert Time	t_loss_assert		100	us	Maximum value designed to support telecom applications
Receiver Loss of Signal De-Assert Time	t_loss_deassert		100	us	Maximum value designed to support telecom applications
Global Alarm Assert Delay Time	GLB_ALRMn_assert		150	ms	This is a logical “OR” of Associated MDIO alarm& status registers.Please see MDIO document for further details
Global Alarm De-assert Delay Time	GLB_ALRMn_deassert		150	ms	This is a logical “OR” of Associated MDIO alarm& status registers.Please see MDIO document for further details
Management Interface Clock Period	t_prd	250		ns	MDC is 4MHz rate
Host MDIO t_setup	t_setup	10		ns	
Host MDIO t_hold	t_hold	10		ns	
CFP MDIO t_delay	t_delay	0	175	ns	
Initialization time from Reset	t_initialize		2.5	s	
Transmitter Disabled(TX_DIS_asserted)	t_deassert		100	us	Application Specific
Transmitter Enabled(TX_DIS_asserted)	t_assert		100	ms	Value is dependent upon module start-up time.Please See register “Maximum TX-Turn-on Time” in “CFP MSA

PIN#	Name	I/O	Logic	Description	Notes
1	GND				
2	(TX_MCLKn)	O	CML	For optical waveform testing.	

3	(TX_MCLKp)	O	CML	For optical waveform testing.	
4	GND				
5	N.C.				
6	N.C.				
7	3.3V_GND			3.3V Module Supply Voltage Return Ground, can be	
8	3.3V_GND				
9	3.3V				
10	3.3V				
11	3.3V				
12	3.3V				
13	3.3V_GND				
14	3.3V_GND				
15	VND_IO_A	I/O		Module Vendor I/O A.	
16	VND_IO_B	I/O		Module Vendor I/O B.	
17	PRG_CNTL1	I	LVCMOS w/ PUR	Programmable Control 1 set over MDIO	
18	PRG_CNTL2	I	LVCMOS w/ PUR	Programmable Control 1 set over MDIO	
19	PRG_CNTL3	I	LVCMOS w/ PUR	Programmable Control 1 set over MDIO	
20	PRG_ALRM1	O	LVCMOS	Programmable Alarm	
21	PRG_ALRM2	O	LVCMOS	Programmable Alarm	
22	PRG_ALRM3	O	LVCMOS	Programmable Alarm	
23	GND				
24	TX_DIS	I	LVCMOS	Transmitter Disable for all lanes, "1" or NC = transmitter disabled, "0"=	
25	RX_LOS	O	LVCMOS	Receiver Loss of Optical Signal, "1": low optical signal, "0":	
26	MOD_LOPWR	I	LVCMOS w/ PUR	Module Low Power Mode. "1" or NC: module in low power	
27	MOD_ABS	O		Module Absent. "1" or NC: module absent, "0": module present	
28	MOD_RSTn	I	LVCMOS w/ PDR	Module Reset. "0" resets the module, "1" or NC = module	
29	GLB_ALRMn	O	LVCMOS	Global Alarm. “0”: alarm condition in any MDIO Alarm register,	
30	GND				

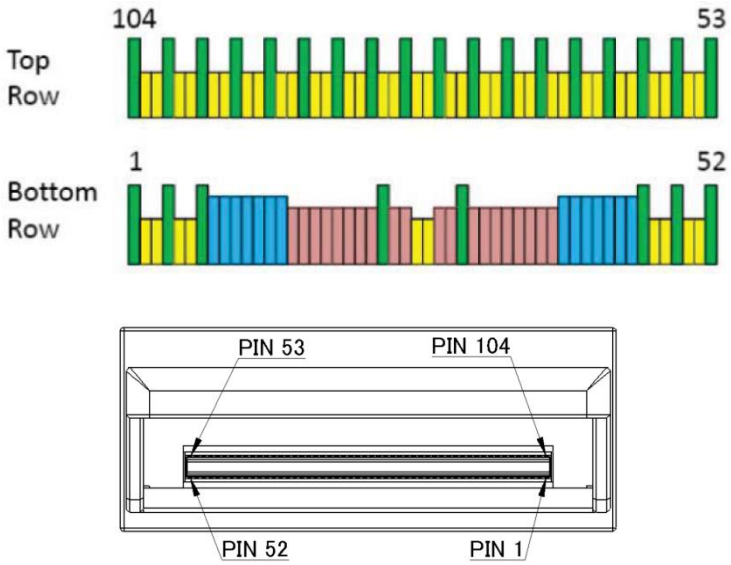
31	MDC	I	1.2V CMOS	Management Data	
32	MDIO	I/O	1.2V CMOS	Management Data I/O	
33	PRTADR0	I	1.2V CMOS	MDIO Physical Port address bit 1	
34	PRTADR1	I	1.2V CMOS	MDIO Physical Port address bit 2	
35	PRTADR2	I	1.2V CMOS	MDIO Physical Port address bit 3	
36	VND_IO_C	I/O		Module Vendor I/O C. Do Not Connect!	
37	VND_IO_D	I/O		Module Vendor I/O D. Do Not Connect!	
38	VND_IO_E	I/O		Module Vendor I/O E. Do Not Connect!	
39	3.3V_GND				
40	3.3V_GND				
41	3.3V				
42	3.3V				
43	3.3V				
44	3.3V				
45	3.3V_GND				
30	GND				
31	MDC	I	1.2V CMOS	Management Data	
32	MDIO	I/O	1.2V CMOS	Management Data I/O	
33	PRTADR0	I	1.2V CMOS	MDIO Physical Port address bit 1	
34	PRTADR1	I	1.2V CMOS	MDIO Physical Port address bit 2	
35	PRTADR2	I	1.2V CMOS	MDIO Physical Port address bit 3	
36	VND_IO_C	I/O		Module Vendor I/O C. Do Not Connect!	
37	VND_IO_D	I/O		Module Vendor I/O D. Do Not Connect!	
38	VND_IO_E	I/O		Module Vendor I/O E. Do Not Connect!	
39	3.3V_GND				
39	3.3V_GND				
40	3.3V_GND				
41	3.3V				
42	3.3V				
43	3.3V				
44	3.3V				
45	3.3V_GND				
46	3.3V_GND				
47	N.C.				
48	N.C.				
49	GND				
50	(RX_MCLKn)	O	CML	For optical waveform testing. Not for	
51	(RX_MCLKp)	O	CML	For optical waveform testing. Not for	

52	GND				
53	GND				
54	N.C.				
55	N.C.				
56	GND				
57	RX0p	O	CML	Output Data	
58	RX0n	O	CML	Inverted Output Data	
59	GND				
60	RX1p	O	CML	Output Data	
61	RX1n	O	CML	Inverted Output Data	
62	GND				
63	N.C.				
64	N.C.				
65	GND				
59	GND				
60	RX1p	O	CML	Output Data	
61	RX1n	O	CML	Inverted Output Data	
62	GND				
63	N.C.				
64	N.C.				
65	GND				
70	RX2n	O	CML	Inverted Output Data	
71	GND				
72	RX3p	O	CML	Output Data	
73	RX3n	O	CML	Inverted Output Data	
74	GND				
75	N.C.				
76	N.C.				
77	GND				
78	NC				
79	NC				
80	GND				
81	N.C.				
82	N.C.				
83	GND				
84	TX0p	I	CML	Input Data	NC
85	TX0n	I	CML	Inverted Input Data	NC
86	GND				

87	TX1p	I	CML	Input Data	NC
88	TX1n	I	CML	Inverted Input Data	NC
89	GND				
90	N.C.				
91	N.C.				
92	GND				
93	N.C.				
94	N.C.				
95	GND				
96	TX2p	I	CML	Input Data	NC
97	TX2n	I	CML	Inverted Input Data	NC
98	GND				
99	TX3p	I	CML	Input Data	NC
100	TX3n	I	CML	Inverted Input Data	NC
101	GND				
102	N.C.				
103	N.C.				
104	GND				

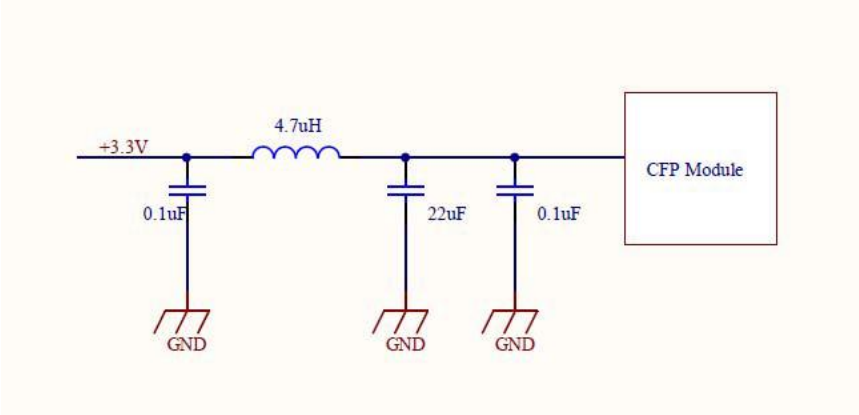
Transmitter and Receiver Monitor Clock Characteristics

		Min	Typ	Max	Unit	Notes
Impedance	Zd	80	100	120	Ω	
Frequency			3220		MHz	1/8 of Network lane rate
Output Differential Voltage	VDIFF	400		1200	mV	Peak to Peak Differential
Clock Duty Cycle		40		60	%	

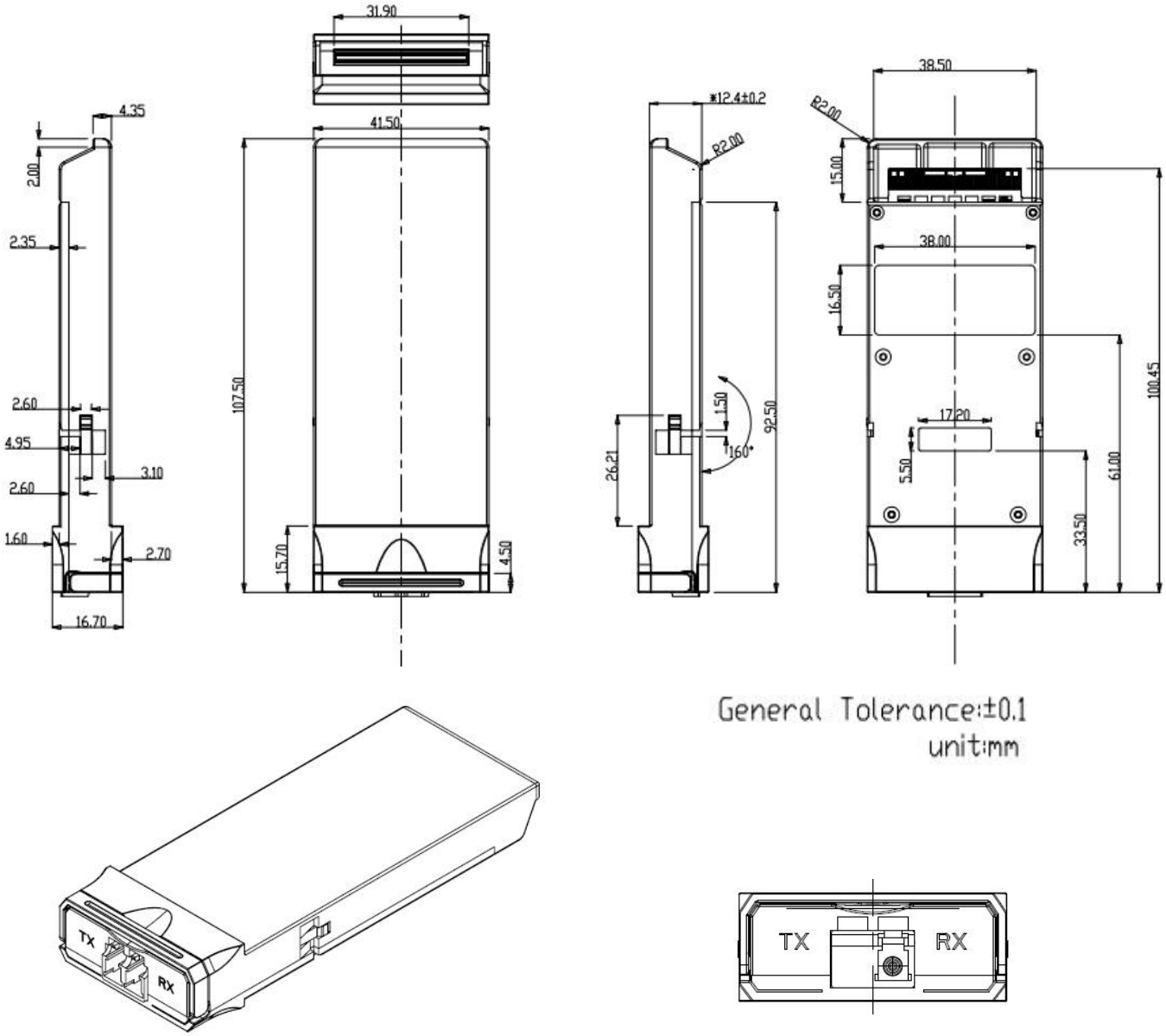


Pad Layout of the CFP2 module

Typical Application Circuit for Power Supply



Mechanical Dimensions



Ordering information

Part Number	Product Description
GF2R-S101-LR4C	CFP2, Receiver only(without TOSA), 100GE/OTU4,10km,100GBASE-LR4

Regulatory Compliance

Feature	Test Method	Performance
Laser Eye Safety	FDA 21 CFR 1040.10 and 1040.11 IEC 60825-1: 1994+ A11: 1996+ A2: 2001 IEC 60825-2: 2004 + A1: 2006 EN 60825-1:1994+A1:2002+A2:2001 EN 60825-2: 2004	Compliant with Class 1 laser product
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883E Method 3015.7 Human Body Model	Class 1 (>1.5kV)
Electrostatic Discharge (ESD) Immunity	IEC 61000-4-2: 2001	Class 2 (>4.0kV)
Electromagnetic Interference (EMI)	FCC Part 15 Subpart J Class B CISPR22:1997+A1:2000+A2:2002, Class B EN55022:1998+A1:2000+A2:2003, Class B	Compliant with standards

Important Notice

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E-mail: sales@gigalight.com.cn
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