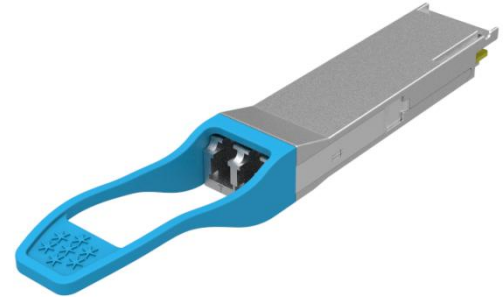


GIGALIGHT Multi-rate 100G QSFP28 LR4 Optical Transceiver Module P/N: GQS-SPO111-LR4C

Features

- ◆ 4 channels full-duplex transceiver modules
- ◆ Transmission data rate up to 28Gbps per channel
- ◆ 4 x 28Gb/s DFB-based LAN-WDM Cooling transmitter
- ◆ 4 channels PIN ROSA
- ◆ Internal CDR circuits on both receiver and transmitter channels
- ◆ Low power consumption <3.5W
- ◆ Hot Pluggable QSFP form factor
- ◆ Up to reach 10km for G.652 SMF
- ◆ Duplex LC receptacles
- ◆ Operating case temperature 0°C to +70°C
- ◆ 3.3V power supply voltage
- ◆ RoHS 6 compliant(lead free)



Applications

- ◆ IEEE 802.3ba 100GBASE LR4
- ◆ OTN OTU4 and 100GE

Description

This product is a 100Gb/s transceiver module designed for optical communication applications compliant to 100GBASE-LR4 of the IEEE P802.3ba standard and OTU4 4I1-9D1F requirements specified in ITU-T Recommendations G.959.1/G.709 and Supplement 39(G.sup39). The module converts 4 input channels of 28Gb/s electrical data to 4 channels of LAN WDM optical signals and then multiplexes them into a single channel for 100Gb/s optical transmission. Reversely on the receiver side, the module de-multiplexes a 100Gb/s optical input into 4 channels of LAN WDM optical signals and then converts them to 4 output channels of electrical data.

The central wavelengths of the 4 LAN WDM channels are 1295.56, 1300.05, 1304.58 and 1309.14 nm as members of the LAN WDM wavelength grid defined in IEEE 802.3ba. The high performance cooled LAN WDM DFB transmitters and high sensitivity PIN receivers provide superior performance for 100Gigabit Ethernet applications up to 10km links and compliant to optical interface with IEEE802.3ba Clause 88 100GBASE-LR4 requirements.

The product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP+ Multi-Source Agreement (MSA). It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference.

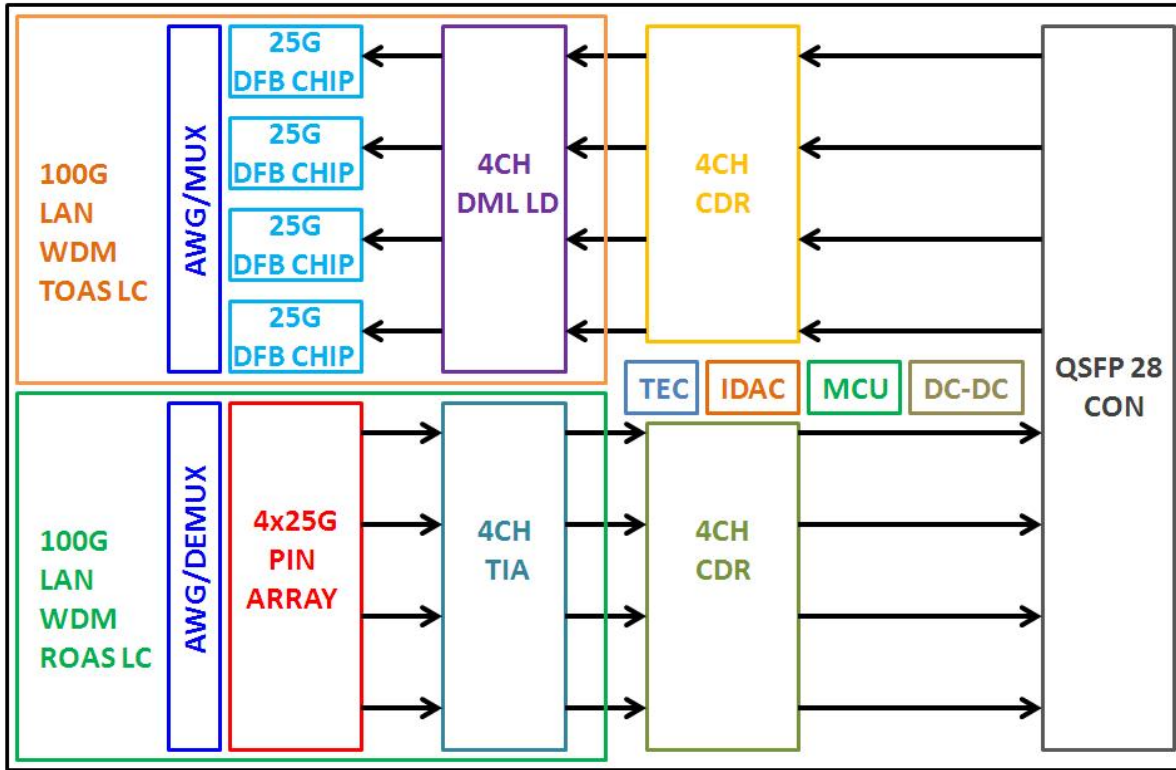


Figure1. Module Block Diagram

Absolute Maximum Ratings

| Parameter | Symbol | Min | Max | Unit |
|-----------------------------|--------|------|---------|------|
| Supply Voltage | Vcc | -0.3 | 3.6 | V |
| Input Voltage | Vin | -0.3 | Vcc+0.3 | V |
| Storage Temperature | Tst | -20 | 85 | °C |
| Case Operating Temperature | Top | 0 | 70 | °C |
| Humidity(non-condensing) | Rh | 5 | 85 | % |
| Damage Threshold, each Lane | TH | 5.5 | | dBm |

Recommended Operating Conditions

| Parameter | Symbol | Min | Typical | Max | Unit |
|----------------------------|--------|-------|---------|------|------|
| Supply Voltage | Vcc | 3.13 | 3.3 | 3.47 | V |
| Operating Case temperature | Tca | 0 | | 70 | °C |
| Data Rate Per Lane | fd | | | 28 | Gbps |
| Humidity | Rh | 5 | | 85 | % |
| Power Dissipation | P | | | 3.5 | W |
| Link Distance with G.652 | D | 0.002 | | 10 | km |

Electrical Specifications

| Parameter | Symbol | Min | Typical | Max | Unit |
|--|------------------|------|---------|------|------|
| Power Consumption | P | | | 3.5 | W |
| Supply Current | I _{cc} | | | 1.06 | A |
| Transceiver Power-on Initialization Time | | | | 2000 | ms |
| Transmitter(each Lane) | | | | | |
| Single-ended Input Voltage Tolerance | | -0.3 | | 4.0 | V |
| AC Common Mode Input Voltage Tolerance | | 15 | | | mV |
| Differential Input Voltage | | 50 | | | mVpp |
| Differential Input Voltage Swing | V _{in} | | | 900 | mVpp |
| Differential Input Impedance | Z _{in} | 90 | 100 | 110 | Ohm |
| Receiver(each Lane) | | | | | |
| Single-ended Output Voltage | | -0.3 | | 4.0 | V |
| AC Common Mode Output Voltage | | | | 7.5 | mV |
| Differential Output Voltage Swing | V _{out} | 300 | | 850 | mVpp |
| Differential Output Impedance | Z _{out} | 90 | 100 | 110 | Ohm |

Note:

Power-on Initialization Time is the time from when the power supply voltages reach and remain above the minimum recommended operating supply voltages to the time when the module is fully functional.

Optical Characteristics

Table 3 - Optical Characteristics 100GBASE-LR4

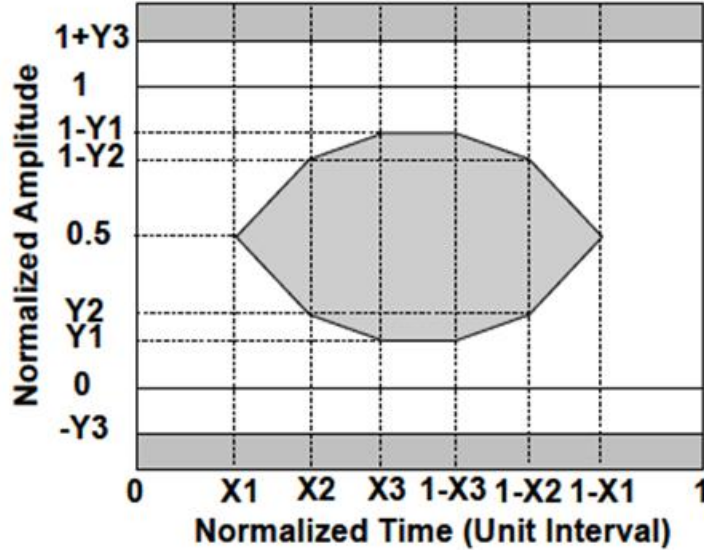
| QSFP28 100GBASE-LR4 | | | | | | |
|---------------------------------|------------------|---------|---------|---------|------|-------|
| Parameter | Symbol | Min | Typical | Max | Unit | Notes |
| Lane Wavelength | L0 | 1294.53 | 1295.56 | 1296.59 | nm | |
| | L1 | 1299.02 | 1300.05 | 1301.09 | nm | |
| | L2 | 1303.54 | 1304.58 | 1305.63 | nm | |
| | L3 | 1308.09 | 1309.14 | 1310.19 | nm | |
| Transmitter | | | | | | |
| SMSR | SMSR | 30 | | | dB | |
| Total Average Launch Power | P _T | | | 10.5 | dBm | |
| Average Launch Power, each Lane | P _{AVG} | -4.3 | | 4.5 | dBm | |

| | | | | | | |
|--|---------------|------------------------------------|-----|------|------|---|
| OMA, each Lane | P_{OMA} | -1.3 | | 4.5 | dBm | 1 |
| Difference in Launch Power | $P_{tx,diff}$ | | | 5 | dB | |
| Launch Power in OMA | | -2.3 | | | dBm | |
| TDP, each Lane | TDP | | | 2.2 | dB | |
| Extinction Ratio | ER | 4 | | | dB | |
| RIN_{20OMA} | RIN | | | -130 | dB/H | |
| Optical Return Loss | TOL | | | 20 | dB | |
| Transmitter Reflectance | R_T | | | -12 | dB | |
| Eye Mask coordinates: X1, X2, X3, Y1, Y2, Y3 | | {0.25, 0.4, 0.45, 0.25, 0.28, 0.4} | | | | 2 |
| Average Launch Power OFF | P_{off} | | | -30 | dBm | |
| Receiver | | | | | | |
| Damage Threshold, each Lane | TH_d | 5.5 | | | dBm | 3 |
| Total Average Receive | | | | 10.5 | dBm | |
| Average Receive Power, each Lane | | -10.6 | | 4.5 | dBm | |
| Receive Power (OMA), each Lane | | | | 4.5 | dBm | |
| Receiver Sensitivity (OMA), each Lane | SEN | | | -8.6 | dBm | |
| Stressed Receiver Sensitivity (OMA), each Lane | | | | -6.8 | dBm | 4 |
| Difference in Receive Power between any Two Lanes (OMA) | $P_{rx,diff}$ | | | 5.5 | dB | |
| LOS Assert | LOSA | | -18 | | dBm | |
| LOS Deassert | LOSD | | -15 | | dBm | |
| LOS Hysteresis | LOSH | 0.5 | | | dB | |
| Receiver Electrical 3 dB upper Cutoff Frequency, each Lane | F_c | | | 31 | GHz | |

| Conditions of Stress Receiver Sensitivity Test (Note 5) | | | | | | |
|---|--|--|------|--|----|---|
| Vertical Eye Closure Penalty, each Lane | | | 1.8 | | dB | 5 |
| Stressed Eye J2 Jitter, each Lane | | | 0.3 | | UI | |
| Stressed Eye J9 Jitter, each Lane | | | 0.47 | | UI | |

Note:

1. Even if the TDP < 1 dB, the OMA min must exceed the minimum value specified here.
2. See Figure 4 below.
3. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.
4. Measured with conformance test signal at receiver input for BER = 1×10^{-12} .
5. Vertical eye closure penalty and stressed eye jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.



OTU4 4I1-9D1F Operation

| QSFP28 100GBASE-LR4 | | | | | | |
|-----------------------------|--------|---------|---------------------|---------|------|-------|
| Parameter | Symbol | Min | Typical | Max | Unit | Notes |
| Signaling Speed per Channel | | | 27.9525+/- 20ppm | | GBd | 1 |
| Lane Wavelength | L0 | 1294.53 | 1295.56 | 1296.59 | nm | |

| | | | | | | |
|---|---------------|------------------------------------|---------------------|---------|-----|---|
| | L1 | 1299.02 | 1300.05 | 1301.09 | nm | |
| | L2 | 1303.54 | 1304.58 | 1305.63 | nm | |
| | L3 | 1308.09 | 1309.14 | 1310.19 | nm | |
| Transmitter | | | | | | |
| Total Average Launch Power | P_T | | | 10 | dBm | |
| Average Launch Power, each Lane | P_{AVG} | -0.6 | | 4.0 | dBm | |
| Difference in Launch Power | $P_{tx,diff}$ | | | 5 | dB | |
| Extinction Ratio | ER | 4 | | 6.5 | dB | |
| Optical Return Loss | TOL | | | 20 | dB | |
| Transmitter Reflectance | R_T | | | -12 | dB | |
| Eye Mask coordinates: X1, X2, X3, Y1, Y2, Y3 | | {0.25, 0.4, 0.45, 0.25, 0.28, 0.4} | | | | 2 |
| Average Launch Power OFF | P_{off} | | | -30 | dBm | |
| Receiver | | | | | | |
| Signaling Speed per Channel | | | 27.9525+/- 20ppm | | GBd | 3 |
| Total Average Receive | | | | 10 | dBm | |
| Average Receive Power, each Lane | | -6.9 | | 4.0 | dBm | 4 |
| Optical Path Penalty | OPP | | | 1.5 | dBm | |
| Equivalent Sensitivity, each Lane | SEN | | | -8.4 | dBm | 4 |
| LOS Assert | LOSA | | | -11.6 | dBm | |
| LOS Deassert | LOSD | | | -13.6 | dBm | |
| LOS Hysteresis | LOSH | 0.5 | | | dB | |

Notes:

1. Transmitter consists of 4 lasers operating at 27.95G/s each.
2. Hit ratio 5×10^{-5} .
3. Receiver consists of 4 photodetectors operating at 27.95Gb/s each.
4. Specified at a BER of 10^{-6} (Pre-FEC),per ITU-T G.sup39.

Pin Descriptions

| Pin | Logic | Symbol | Name/Description | Ref. |
|-----|------------|---------|---|------|
| 1 | | GND | Module Ground | 1 |
| 2 | CML-I | Tx2- | Transmitter inverted data input | |
| 3 | CML-I | Tx2+ | Transmitter non-inverted data input | |
| 4 | | GND | Module Ground | 1 |
| 5 | CML-I | Tx4- | Transmitter inverted data input | |
| 6 | CML-I | Tx4+ | Transmitter non-inverted data input | |
| 7 | | GND | Module Ground | 1 |
| 8 | LVTTL-I | MODSEIL | Module Select | 2 |
| 9 | LVTTL-I | ResetL | Module Reset | 2 |
| 10 | | VCCRx | +3.3v Receiver Power Supply | |
| 11 | LVCMOS-I | SCL | 2-wire Serial interface clock | 2 |
| 12 | LVCMOS-I/O | SDA | 2-wire Serial interface data | 2 |
| 13 | | GND | Module Ground | 1 |
| 14 | CML-O | RX3+ | Receiver non-inverted data output | |
| 15 | CML-O | RX3- | Receiver inverted data output | |
| 16 | | GND | Module Ground | 1 |
| 17 | CML-O | RX1+ | Receiver non-inverted data output | |
| 18 | CML-O | RX1- | Receiver inverted data output | |
| 19 | | GND | Module Ground | 1 |
| 20 | | GND | Module Ground | 1 |
| 21 | CML-O | RX2- | Receiver inverted data output | |
| 22 | CML-O | RX2+ | Receiver non-inverted data output | |
| 23 | | GND | Module Ground | 1 |
| 24 | CML-O | RX4- | Receiver inverted data output | |
| 25 | CML-O | RX4+ | Receiver non-inverted data output | |
| 26 | | GND | Module Ground | 1 |
| 27 | LVTTL-O | ModPrsL | Module Present, internal pulled down to GND | |
| 28 | LVTTL-O | IntL | Interrupt output, should be pulled up on host board | 2 |
| 29 | | VCCTx | +3.3v Transmitter Power Supply | |
| 30 | | VCC1 | +3.3v Power Supply | |
| 31 | LVTTL-I | LPMODE | Low Power Mode | 2 |
| 32 | | GND | Module Ground | 1 |
| 33 | CML-I | Tx3+ | Transmitter non-inverted data input | |
| 34 | CML-I | Tx3- | Transmitter inverted data input | |
| 35 | | GND | Module Ground | 1 |
| 36 | CML-I | Tx1+ | Transmitter non-inverted data input | |
| 37 | CML-I | Tx1- | Transmitter inverted data input | |
| 38 | | GND | Module Ground | 1 |

Notes:

1. Module circuit ground is isolated from module chassis ground within the module.
2. Open collector; should be pulled up with 4.7k – 10k ohms on host board to a voltage between 3.15V and 3.6V.

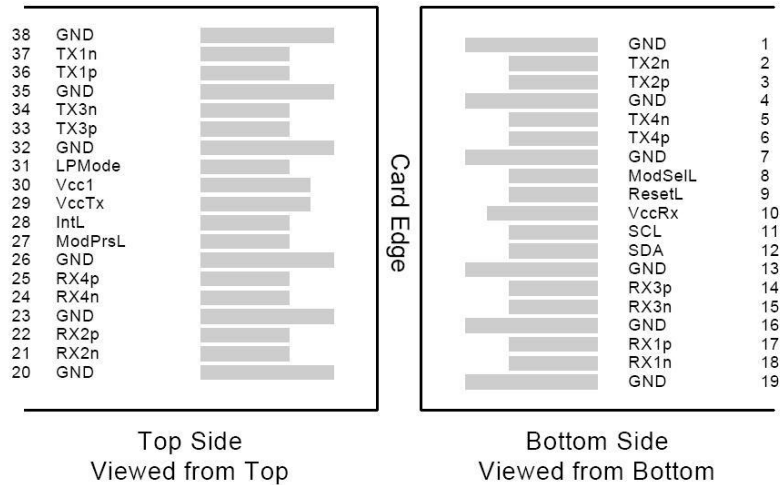


Figure 2. Electrical Pin-out Details

ModSelL Pin

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP modules on a single 2-wire interface bus. When the ModSelL is “High”, the module will not respond to any 2-wire interface communication from the host. ModSelL has an internal pull-up in the module.

ResetL Pin

Reset. LPMode_Reset has an internal pull-up in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_{Reset_init}) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_{init}) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_{init}) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module will post this completion of reset interrupt without requiring a reset.

LPMode Pin

Gigalight QSFP28 SR4 operate in the low power mode (less than 1.5 W power consumption)
This pin active high will decrease power consumption to less than 1W.

ModPrsL Pin

ModPrsL is pulled up to Vcc on the host board and grounded in the module. The ModPrsL is asserted “Low” when the module is inserted and deasserted “High” when the module is physically absent from the host connector.

IntL Pin

IntL is an output pin. When “Low”, it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt by using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled up to Vcc on the host board.

Power Supply Filtering

The host board should use the power supply filtering shown in Figure3.

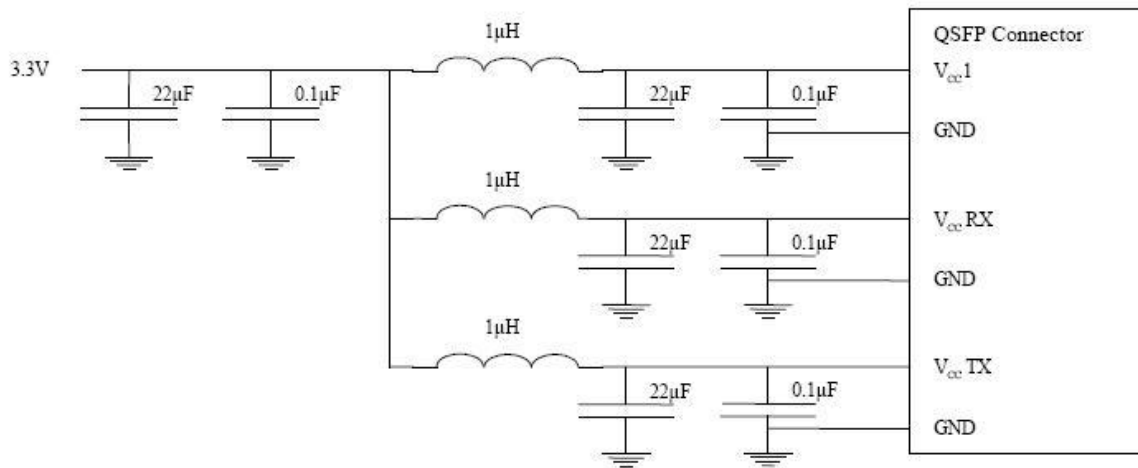


Figure3. Host Board Power Supply Filtering

DIAGNOSTIC MONITORING INTERFACE (OPTIONAL)

The following digital diagnostic characteristics are defined over the normal operating conditions unless otherwise specified.

| Parameter | Symbol | Min | Max | Units | Notes |
|---|--------------|------|-----|-------|----------------------------------|
| Temperature monitor absolute error | DMI_Temp | -3 | +3 | deg C | Over operating temperature range |
| Supply voltage monitor absolute error | DMI_VCC | -0.1 | 0.1 | V | Over full operating range |
| Channel RX power monitor absolute error | DMI_RX_Ch | -2 | 2 | dB | 1 |
| Channel Bias current monitor | DMI_Ibias_Ch | -10% | 10% | mA | |
| Channel TX power monitor absolute error | DMI_TX_Ch | -2 | 2 | dB | 1 |

Notes:

Due to measurement accuracy of different single mode fibers, there could be an additional +/- 1 dB fluctuation, or a +/- 3 dB total accuracy.

Digital diagnostics monitoring function is available on all Gigalight QSFP28 LR4. A 2-wire serial interface

provides user to contact with module.

The structure of the memory is shown in Figure 5. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages. This structure permits timely access to addresses in the lower page, such as Interrupt Flags and Monitors. Less time critical time entries, such as serial ID information and threshold settings, are available with the Page Select function.

The interface address used is A0xh and is mainly used for time critical data like interrupt handling in order to enable a one-time-read for all data related to an interrupt situation. After an interrupt, IntL, has been asserted, the host can read out the flag field to determine the affected channel and type of flag.

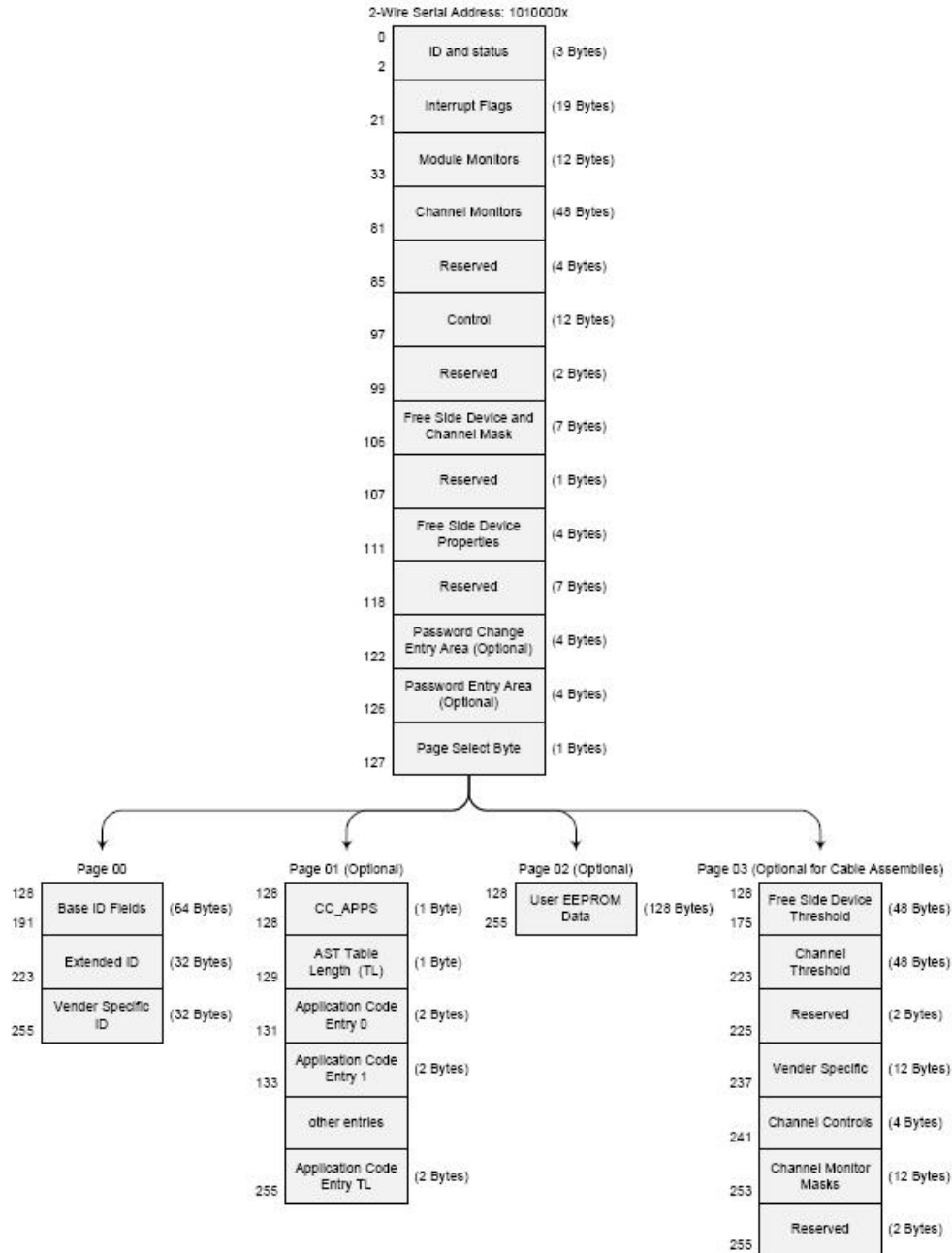


Figure5. QSFP Memory Map

| Byte Address | Description | Type |
|--------------|------------------------------------|------------|
| 0 | Identifier (1 Byte) | Read Only |
| 1-2 | Status (2 Bytes) | Read Only |
| 3-21 | Interrupt Flags (31 Bytes) | Read Only |
| 22-33 | Module Monitors (12 Bytes) | Read Only |
| 34-81 | Channel Monitors (48 Bytes) | Read Only |
| 82-85 | Reserved (4 Bytes) | Read Only |
| 86-97 | Control (12 Bytes) | Read/Write |
| 98-99 | Reserved (2 Bytes) | Read/Write |
| 100-106 | Module and Channel Masks (7 Bytes) | Read/Write |
| 107-118 | Reserved (12 Bytes) | Read/Write |
| 119-122 | Reserved (4 Bytes) | Read/Write |
| 123-126 | Reserved (4 Bytes) | Read/Write |
| 127 | Page Select Byte | Read/Write |

Figure6. Low Memory Map

| Byte Address | Description | Type |
|--------------|------------------------------|------------|
| 128-175 | Module Thresholds (48 Bytes) | Read Only |
| 176-223 | Reserved (48 Bytes) | Read Only |
| 224-225 | Reserved (2 Bytes) | Read Only |
| 226-239 | Reserved (14 Bytes) | Read/Write |
| 240-241 | Channel Controls (2 Bytes) | Read/Write |
| 242-253 | Reserved (12 Bytes) | Read/Write |
| 254-255 | Reserved (2 Bytes) | Read/Write |

Figure7. Page 03 Memory Map

| Address | Name | Description |
|---------|---|--|
| 128 | Identifier (1 Byte) | Identifier Type of serial transceiver |
| 129 | Ext. Identifier (1 Byte) | Extended identifier of serial transceiver |
| 130 | Connector (1 Byte) | Code for connector type |
| 131-138 | Transceiver (8 Bytes) | Code for electronic compatibility or optical compatibility |
| 139 | Encoding (1 Byte) | Code for serial encoding algorithm |
| 140 | BR, nominal (1 Byte) | Nominal bit rate, units of 100 Mbits/s |
| 141 | Extended RateSelect Compliance (1 Byte) | Tags for Extended RateSelect compliance |
| 142 | Length SMF (1 Byte) | Link length supported for SM fiber in km |
| 143 | Length E-50 μm (1 Byte) | Link length supported for EBW 50/125 μm fiber, units of 2 m |
| 144 | Length 50 μm (1 Byte) | Link length supported for 50/125 μm fiber, units of 1 m |
| 145 | Length 62.5 μm (1 Byte) | Link length supported for 62.5/125 μm fiber, units of 1 m |
| 146 | Length copper (1 Byte) | Link length supported for copper, units of 1 m |
| 147 | Device Tech (1 Byte) | Device technology |
| 148-163 | Vendor name (16 Bytes) | QSFP vendor name (ASCII) |
| 164 | Extended Transceiver (1 Byte) | Extended Transceiver Codes for InfiniBand [†] |
| 165-167 | Vendor OUI (3 Bytes) | QSFP vendor IEEE vendor company ID |
| 168-183 | Vendor PN (16 Bytes) | Part number provided by QSFP vendor (ASCII) |
| 184-185 | Vendor rev (2 Bytes) | Revision level for part number provided by vendor (ASCII) |
| 186-187 | Wavelength (2 Bytes) | Nominal laser wavelength (Wavelength = value / 20 in nm) |
| 188-189 | Wavelength Tolerance (2 Bytes) | Guaranteed range of laser wavelength (+/- value) from Nominal wavelength (Wavelength Tol. = value / 200 in nm) |
| 190 | Max Case Temp (1 Byte) | Maximum Case Temperature in Degrees C |
| 191 | CC_BASE (1 Byte) | Check code for Base ID fields (addresses 128-190) |
| 192-195 | Options (4 Bytes) | Rate Select, TX Disable, TX Fault, LOS |
| 196-211 | Vendor SN (16 Bytes) | Serial number provided by vendor (ASCII) |
| 212-219 | Date code (8 Bytes) | Vendor's manufacturing date code |
| 220 | Diagnostic Monitoring Type (1 Byte) | Indicates which type of diagnostic monitoring is implemented |
| 221 | Enhanced Options (1 Byte) | Indicates which optional enhanced features are implemented |
| 222 | Reserved (1 Byte) | Reserved |
| 223 | CC_EXT | Check code for the Extended ID Fields (addresses 192-222) |
| 224-255 | Vendor Specific (32 Bytes) | Vendor Specific EEPROM |

Figure8. Page 00 Memory Map

Page02 is User EEPROM and its format decided by user.

The detail description of low memory and page00.page03 upper memory please see SFF-8436 document.

Timing for Soft Control and Status Functions

| Parameter | Symbol | Max | Unit | Conditions |
|--|--------------|------|------|---|
| Initialization Time | t_init | 2000 | ms | Time from power on ¹ , hot plug or rising edge of Reset until the module is fully functional ² |
| Reset Init Assert Time | t_reset_init | 2 | μs | A Reset is generated by a low level longer than the minimum reset pulse time present on the ResetL pin. |
| Serial Bus Hardware Ready Time | t_serial | 2000 | ms | Time from power on ¹ until module responds to data transmission over the 2-wire serial bus |
| Monitor Data Ready Time | t_data | 2000 | ms | Time from power on ¹ to data not ready, bit 0 of Byte 2, deasserted and IntL asserted |
| Reset Assert Time | t_reset | 2000 | ms | Time from rising edge on the ResetL pin until the module is fully functional ² |
| LPMODE Assert Time | ton_LPMODE | 100 | μs | Time from assertion of LPMODE (Vin:LPMODE = Vih) until module power consumption enters lower Power Level |
| IntL Assert Time | ton_IntL | 200 | ms | Time from occurrence of condition triggering IntL until Vout:IntL = Vol |
| IntL Deassert Time | toff_IntL | 500 | μs | Time from clear on read ³ operation of associated flag until Vout:IntL = Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits. |
| Rx LOS Assert Time | ton_los | 100 | ms | Time from Rx LOS state to Rx LOS bit set and IntL asserted |
| Tx Fault Assert Time | ton_Txfault | 200 | ms | Time from Tx Fault state to Tx Fault bit set and IntL asserted |
| Flag Assert Time | ton_flag | 200 | ms | Time from occurrence of condition triggering flag to associated flag bit set and IntL asserted |
| Mask Assert Time | ton_mask | 100 | ms | Time from mask bit set ⁴ until associated IntL assertion is inhibited |
| Mask Deassert Time | toff_mask | 100 | ms | Time from mask bit cleared ⁴ until associated IntL operation resumes |
| ModSelL Assert Time | ton_ModSelL | 100 | μs | Time from assertion of ModSelL until module responds to data transmission over the 2-wire serial bus |
| ModSelL Deassert Time | toff_ModSelL | 100 | μs | Time from deassertion of ModSelL until the module does not respond to data transmission over the 2-wire serial bus |
| Power_over-ride or Power-set Assert Time | ton_Pdown | 100 | ms | Time from P_Down bit set ⁴ until module power consumption enters lower Power Level |
| Power_over-ride or Power-set Deassert Time | toff_Pdown | 300 | ms | Time from P_Down bit cleared ⁴ until the module is fully functional ³ |

Note:

1. Power on is defined as the instant when supply voltages reach and remain at or above the minimum specified value.
2. Fully functional is defined as IntL asserted due to data not ready bit, bit 0 byte 2 deasserted.
3. Measured from falling clock edge after stop bit of read transaction.
4. Measured from falling clock edge after stop bit of write transaction.

Figure9. Timing Specifications

Mechanical Dimensions

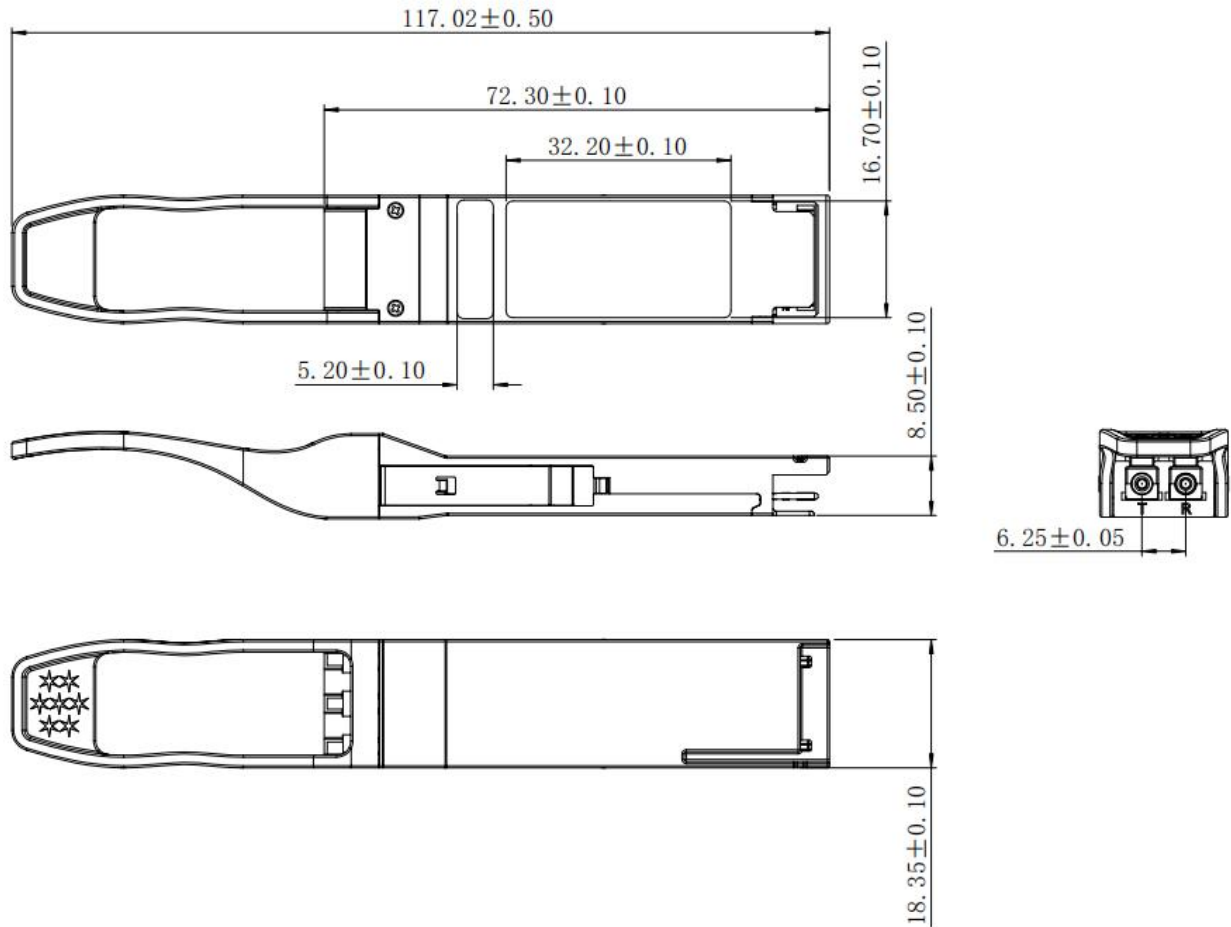


Figure10. Mechanical Specifications

Ordering information

| Part Number | Product Description |
|-----------------|---|
| GQS-SPO111-LR4C | QSFP28, 100GBASE-LR4 and OTU4, LAN_WDM 10km |

References

1. SFF-8436 QSFP+
2. Ethernet 100GBASE-LR4
3. OTN OTU4

ESD

This transceiver is specified as ESD threshold 1kV for SFI pins and 2kV for all other electrical input pins,

tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

Laser Safety

This is a Class 1 Laser Product according to IEC 60825-1:2007. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007).

Important Notice

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