

GIGALIGHT 40G QSFP+ LR4 10km GQS-SPO400-LR4CC,Pull-Tab

Features

- ◆ Transmission data rate up to 11.2Gbps per channel
- ◆ QSFP+ MSA compliant
- ◆ Compliant to IEEE 802.3ba specification for 40GBASE-LR4 links
- ◆ 4 CWDM un-cooled DFB lasers, using ITU G.694.2 wavelength grid at 1270, 1290, 1310, and 1330nm
- ◆ High Sensitivity PIN-TIA with optical DEMUX
- ◆ Up to 10km reach over standard single mode fiber
- ◆ Compliant with QDR/DDR Infiniband data rates
- ◆ Hot pluggable electrical interface
- ◆ Power consumption < 3.5W
- ◆ Operating case temperature 0°C to +70°C
- ◆ 3.3V power supply
- ◆ RoHS 6 compliant (lead free)



Applications

- ◆ 40G Ethernet
- ◆ Infiniband QDR and DDR interconnects
- ◆ Client-side 40G Telecom connections

Description

The GQS-SPO400-LR4CC is a 4x10G hot pluggable optical transceiver. The Gigalight technology enables the integration of 4 transmitters, 4 receivers and an optical MUX/DeMUX into a small form factor package that delivers a 40 Gbps data link in a compact QSFP footprint. The optical connectivity is based on two SMF LC connectors, one for Tx and one for Rx. The Tx and Rx each consist of 4 10Gb/s CWDM channels, whose wavelengths are in the 1300nm range. The QSFP-LR transceiver is designed for applications based on the QSFP MSA, IEEE 802.3ba and 40GBASE-LR4 requirements of up to 10km reach.

Functional Block Diagram

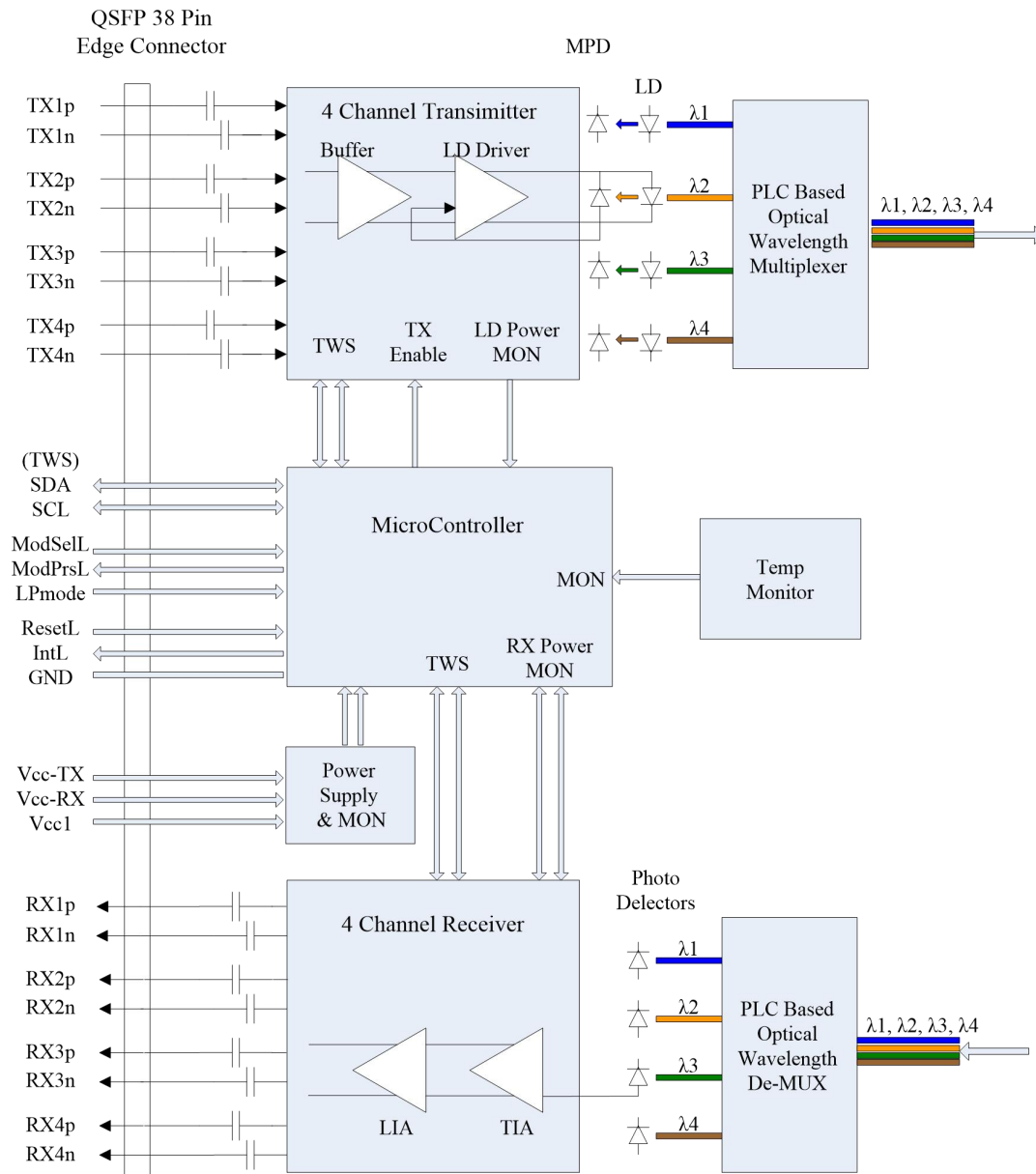


Figure 1: Functional Block Diagram

Absolute Maximum Ratings

| Parameter | Symbol | Min | Max | Unit |
|-----------|--------|-----|-----|------|
|-----------|--------|-----|-----|------|

| | | | | |
|---|--|-----------------------------|-----|-----|
| Supply Voltage | V _{CC-Tx} V _{CC-Rx} V _{CC1} | -0.5 | 3.6 | V |
| Storage Temperature Range | T _{STG} | -40 | +85 | °C |
| Maximum Average Input Optical Power per lane (Damage Threshold) | P _{IN} | 3.4 | | dBm |
| Relative Humidity | RH | 10% to 90% (non-condensing) | | |

Operating Conditions

| Parameter | Symbol | Min | Max | Unit |
|----------------------------|--|-----|-----|------|
| Supply Voltage | V _{CC-Tx} V _{CC-Rx} V _{CC1} | 3.1 | 3.5 | V |
| Operating Case temperature | T _{CASE} | 0 | 70 | °C |
| Power Consumption | P _{DISS} | | 3.5 | W |
| SMF Link Length | L _{KM} | | 10 | km |

High Speed Electrical Specifications

| Parameter | Min | Typical | Max | Units |
|---|-----|---------|------|-------|
| General | | | | |
| Supply Voltage | 3.1 | 3.3 | 3.5 | Volts |
| Supply Current | | | 1.0 | Amps |
| Maximum Power Consumption | | | 3.5 | Watts |
| Maximum Power Consumption – LP Mode | | | 1.5 | Watts |
| Signaling Speed Per Channel | | 10.3125 | | Gb/s |
| Transmitter | | | | |
| Transmitter Differential Input Impedance | | 100 | | ohms |
| Transmitter Differential Input Voltage | 120 | | 1200 | mVpp |
| Transmitter Signaling Speed Operating Range | | ±20 | | ppm |
| Receiver | | | | |
| Differential Output impedance | | 100 | | ohms |
| Receiver Signaling Speed Operating Range | | ±100 | | ppm |
| Differential output voltage | | 300 | 850 | mV |
| Rise Time | | | 60 | ps |

| | | | | |
|-----------|--|--|----|----|
| Fall Time | | | 60 | ps |
|-----------|--|--|----|----|

Optical Characteristics

Transmitter Specifications – Optical

| Parameter | Min | Typical | Max | Unit |
|---|---|------------------------------|--------------------------------------|-------|
| Lane Wavelength Range | 1264.5 1284.5 1304.5 1324.5 | 1270 1290 1310 1330 | 1277.5 1297.5 1317.5 1337.5 | nm |
| Data Rate Per Lane | | 10.3125 | | Gb/s |
| Average Optical power per lane | -7.6 | | 2.3 | dBm |
| Total Average Launch power | | | 8.3 | dBm |
| Optical Modulation Amplitude (OMA), each lane | -4 | | 3.5 | dBm |
| Extinction Ratio | 3.5 | | | dB |
| Difference in launch power between any two lanes | | | 6.5 | dB |
| Relative Intensity Noise (RIN) | | | -128 | dB/Hz |
| Launch Power in OMA minus TDP, each lane | -4.8 | | | dBm |
| Transmitter and dispersion penalty (TDP), each lane | | | 2.6 | dB |
| Side-Mode Suppression Ratio (SMSR) | 30 | | | dB |
| Average Launch Power per lane @ TX off state | | | -30 | dBm |
| Transmitter Reflectance | | | -12 | dB |
| Optical return loss tolerance | | | 20 | dB |
| Transmitter Eye Mask definition: X1, X2, X3, Y1, Y2, Y3 | Compliant with 802.3ba standard {0.25, 0.4, 0.45, 0.25, 0.28, 0.4} | | | |
| Eye Mask Criteria | 5% mask margin over specified ranges of temperature, voltage and power supply noise at end of life. | | | |

Receiver Specifications – Optical

| Parameter | Min | Typical | Max | Unit |
|-----------|-----|---------|-----|------|
|-----------|-----|---------|-----|------|

| | | | | |
|--|--------------------------------------|------------------------------|--------------------------------------|-----|
| Lane Wavelength Range | 1264.5 1284.5 1304.5 1324.5 | 1270 1290 1310 1330 | 1277.5 1297.5 1317.5 1337.5 | nm |
| Damage Threshold | | | 3.4 | dBm |
| Average Receive Power, each lane | -13.7 | | 2.3 | dBm |
| Receive Power, each lane (OMA) | | | 3.5 | dBm |
| Difference in Receive Power between any two lanes (OMA) | | | 7.5 | dB |
| Receiver Reflectance | | | -26 | dB |
| Receiver Sensitivity (OMA) per lane (10.3125Gb/s @ PRBS 2 ³¹ -1 and BER=10 ⁻¹²) | | | -11.5 | dBm |
| Receiver 3 dB electrical upper cutoff frequency, each lane | | | 12.3 | GHz |
| Stressed Receiver Sensitivity (OMA), each lane | | | -9.6 | dBm |
| RX_LOS_Assert Min/Max | -30 | | | dBm |
| RX_LOS_De-Assert Max | | | -14 | dBm |
| RX_LOS_Hysteresis | 0.5 | | | dB |

Recommended Host Board Power Supply Filtering

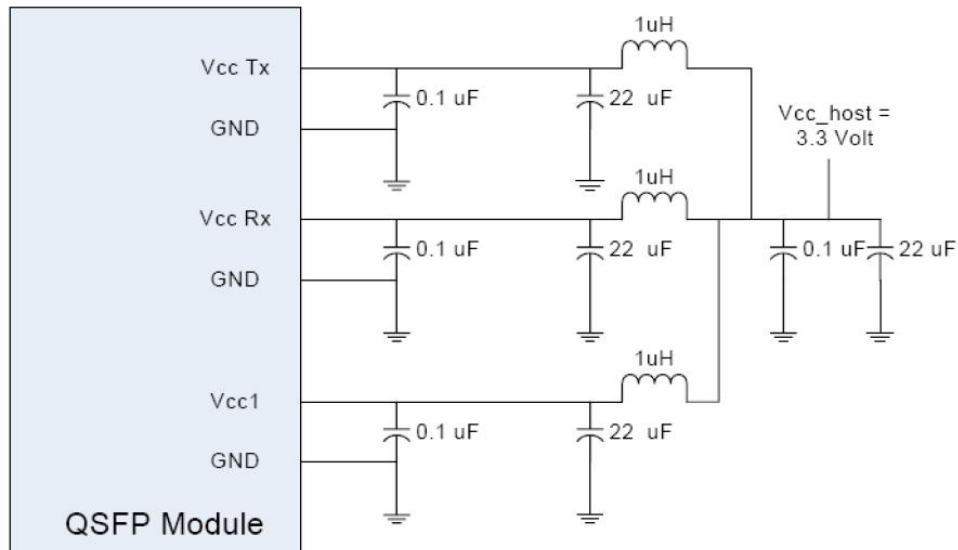


Figure 2. QSFP voltage supply and filtering scheme

Pin Descriptions

| Pin | Logic | Symbol | Name/Description | Ref. |
|-----|-------|--------|------------------|------|
|-----|-------|--------|------------------|------|

| | | | | |
|----|-------------|---------|---|---|
| 1 | | GND | Module Ground | 1 |
| 2 | CML-I | Tx2- | Transmitter inverted data input | |
| 3 | CML-I | Tx2+ | Transmitter non-inverted data input | |
| 4 | | GND | Module Ground | 1 |
| 5 | CML-I | Tx4- | Transmitter inverted data input | |
| 6 | CML-I | Tx4+ | Transmitter non-inverted data input | |
| 7 | | GND | Module Ground | 1 |
| 8 | LVTTL-I | MODSEIL | Module Select | 2 |
| 9 | LVTTL-I | ResetL | Module Reset | 2 |
| 10 | | VCCRx | +3.3v Receiver Power Supply | |
| 11 | LVC MOS-I | SCL | 2-wire Serial interface clock | 2 |
| 12 | LVC MOS-I/O | SDA | 2-wire Serial interface data | 2 |
| 13 | | GND | Module Ground | 1 |
| 14 | CML-O | RX3+ | Receiver non-inverted data output | |
| 15 | CML-O | RX3- | Receiver inverted data output | |
| 16 | | GND | Module Ground | 1 |
| 17 | CML-O | RX1+ | Receiver non-inverted data output | |
| 18 | CML-O | RX1- | Receiver inverted data output | |
| 19 | | GND | Module Ground | 1 |
| 20 | | GND | Module Ground | 1 |
| 21 | CML-O | RX2- | Receiver inverted data output | |
| 22 | CML-O | RX2+ | Receiver non-inverted data output | |
| 23 | | GND | Module Ground | 1 |
| 24 | CML-O | RX4- | Receiver inverted data output | |
| 25 | CML-O | RX4+ | Receiver non-inverted data output | |
| 26 | | GND | Module Ground | 1 |
| 27 | LVTTL-O | ModPrsL | Module Present, internal pulled down to GND | |
| 28 | LVTTL-O | IntL | Interrupt output, should be pulled up on host board | 2 |
| 29 | | VCCTx | +3.3v Transmitter Power Supply | |
| 30 | | VCC1 | +3.3v Power Supply | |
| 31 | LVTTL-I | LPMODE | Low Power Mode | 2 |
| 32 | | GND | Module Ground | 1 |
| 33 | CML-I | Tx3+ | Transmitter non-inverted data input | |
| 34 | CML-I | Tx3- | Transmitter inverted data input | |
| 35 | | GND | Module Ground | 1 |
| 36 | CML-I | Tx1+ | Transmitter non-inverted data input | |
| 37 | CML-I | Tx1- | Transmitter inverted data input | |
| 38 | | GND | Module Ground | 1 |

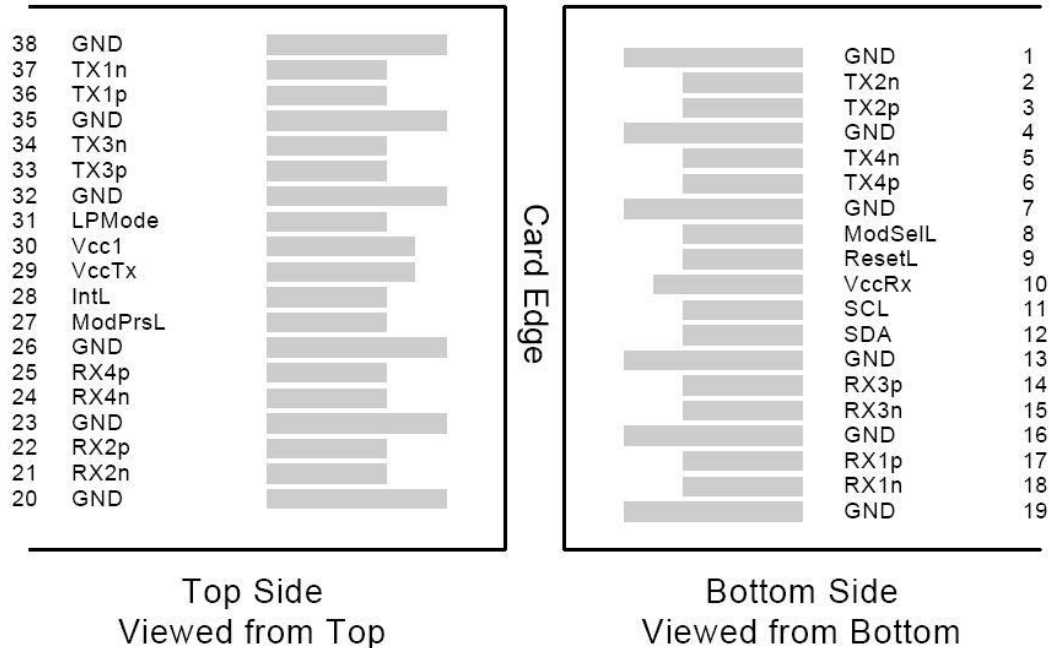
Notes:

1. Module circuit ground is isolated from module chassis ground within the module.
2. Open collector; should be pulled up with 4.7k – 10k ohms on host board to a voltage between 3.15V and

3.6V.

QSFP Edge Connector and Pinout Description

The electrical interface to the transceiver is a 38-pin edge connector. The 38-pins provide high speed data, low speed monitoring and control signals, I²C communication, power and ground connectivity. The top and bottom views of the connector are provided below, as well as a table outlining the contact numbering, symbol and full description.



ModSelL Pin

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP modules on a single 2-wire interface bus. When the ModSelL is “High”, the module will not respond to any 2-wire interface communication from the host.

ModSelL has an internal pull-up in the module.

ResetL Pin

Reset. LPMode_Reset has an internal pull-up in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_{Reset_init}) initiates a complete module reset, returning all user module settings to

their default state. Module Reset Assert Time (t_{init}) starts on the rising edge after the low level on the

ResetL pin is released. During the execution of a reset (t_{init}) the host shall disregard all status bits until the

module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with

the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module will

post this completion of reset interrupt without requiring a reset.

LPMode Pin

Gigalight QSFP PSM LR4 operate in the low power mode (less than 1.5 W power consumption) This pin active high will decrease power consumption to less than 1W.

| LPMode | Power_Override Bit | Power_set Bit | Module Power Allowed |
|--------|--------------------|---------------|----------------------|
| 1 | 0 | X | Low Power (< 1.5W) |
| 0 | 0 | X | High Power (< 3.5W) |
| X | 1 | 1 | Low Power (< 1.5W) |
| X | 1 | 0 | High Power (< 3.5W) |

ModPrsL Pin

ModPrsL is pulled up to Vcc on the host board and grounded in the module. The ModPrsL is asserted “Low”

when the module is inserted and deasserted “High” when the module is physically absent from the host connector.

IntL Pin

IntL is an output pin. When “Low”, it indicates a possible module operational fault or a status critical to the

host system. The host identifies the source of the interrupt by using the 2-wire serial interface. The IntL pin is

an open collector output and must be pulled up to Vcc on the host board.

The timing for QSFP Soft Control and Status Functions are described as follows:

| Parameter | Symbol | Max | Unit | Conditions |
|--------------------------------|--------------|------|------|---|
| Initialization Time | t_init | 2000 | ms | Time from power on ² , hot plug or rising edge of Reset until the module is fully functional ³ This time does not apply to non-Power Level 0 modules in the Low Power State |
| Reset Init Assert Time | t_reset_init | 2 | µs | A Reset is generated by a low level longer than the minimum reset pulse time present on the ResetL pin. |
| Serial Bus Hardware Ready Time | t_serial | 2000 | ms | Time from power on ² until module responds to data transmission over the 2-wire serial bus |
| Monitor Data Ready Time | t_data | 2000 | ms | Time from power on ² to data not ready, bit 0 of Byte 2, deasserted and IntL asserted |
| Reset Assert Time | t_reset | 2000 | ms | Time from rising edge on the ResetL pin until the module is fully functional ³ |
| LPMode Assert Time | ton_LPMode | 100 | µs | Time from assertion of LPMode (Vin:LPMode = Vih) until module power consumption enters lower Power Level 1 |
| LPMode Deassert Time | Toff_LPMode | 300 | ms | Time for deassertion of LPMode (Vin:LPMode=Vil) until module is fully functional ^{3,5} |
| IntL Assert Time | ton_IntL | 200 | ms | Time from occurrence of condition triggering IntL until Vout:IntL = Vol |
| IntL Deassert Time | toff_IntL | 500 | µs | Time from clear on read ⁴ operation of associated flag until Vout:IntL = Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits. |
| Rx LOS Assert Time | ton_los | 100 | ms | Time from Rx LOS state to Rx LOS bit set (value=1b) and IntL asserted |
| Tx Fault Assert Time | ton_Txfault | 200 | ms | Time from Tx Fault state to Tx Fault bit set (value=1b) and IntL asserted |
| Flag Assert Time | ton_flag | 200 | ms | Time from occurrence of condition triggering flag to associated flag bit set (value=1b) and IntL asserted |

| | | | | |
|--|------------|-----|----|---|
| Mask Assert Time | ton_mask | 100 | ms | Time from mask bit set(value=1b) ¹ until associated IntL assertion is inhibited |
| Mask Deassert Time | toff_mask | 100 | ms | Time from mask bit cleared (value=0b) ¹ until associated IntL operation resumes |
| Application or Rate Select Change Time | t_ratesel | 100 | µs | Time from change of state of Application or Rate Select Bit ¹ until transmitter or receiver bandwidth is in conformance with appropriate specification |
| Power_over-ride or Power-set Assert Time | ton_Pdown | 100 | ms | Time from P_Down bit set (value=1b) ¹ until module power consumption enters lower Power Level 1 |
| Power_over-ride or Power-set Deassert Time | toff_Pdown | 300 | ms | Time from P_Down bit cleared(value=0b) ¹ until the module is fully functional ³ |

Note:

1. Measured from falling clock edge after stop bit of read transaction.
2. Power on is defined as the instant when supply voltages reach and remain at or above the minimum level specified value.
3. Fully functional is defined as IntL asserted due to data not ready bit, bit 0 byte 2 deasserted. The module should also meet optical and electrical specifications
4. Measured from falling clock edge after stop bit of write transaction.

Squelch and disable timings are defined in the table below:

| Parameter | Symbol | Max | Unit | Conditions |
|---------------------------------|------------|-----|------|---|
| Rx Squelch Assert Time | ton_Rxsq | 80 | us | Time from loss of Rx input signal until the squelched output condition is reached. |
| Rx Squelch Deassert Time | toff_Rxsq | 80 | us | Time from resumption of Rx input signals until normal Rx output condition is reached. |
| Tx Squelch Assert Time | ton_Txsq | 400 | ms | Time from loss of Tx input signal until the squelched output condition is reached. |
| Tx Squelch Deassert Time | toff_Txsq | 400 | ms | Time from resumption of Tx input signals until normal Tx output condition is reached. |
| Tx Disable Assert Time | ton_txdis | 100 | ms | Time from Tx Disable bit set (value = 1b) ¹ until optical output falls below 10% of nominal |
| Tx Disable Deassert Time | toff_txdis | 400 | ms | Time from Tx Disable bit cleared (value = 0b) ¹ until optical output rises above 90% of nominal |
| Rx Output Disable Assert Time | ton_rxdis | 100 | ms | Time from Rx Output Disable bit set (value = 1b) ¹ until Rx output falls below 10% of nominal |
| Rx Output Disable Deassert Time | toff_rxdis | 100 | ms | Time from Rx Output Disable bit cleared (value = 0b) ¹ until Rx output rises above 90% of nominal |
| Squelch Disable Assert Time | ton_sqdis | 100 | ms | This applies to Rx and Tx Squelch and is the time from bit set (value = 0b) ¹ until squelch functionality is disabled. |
| Squelch Disable Deassert Time | toff_sqdis | 100 | ms | This applies to Rx and Tx Squelch and is the time from bit cleared (value = 0b) ¹ until squelch functionality is enabled |

Note:

1. Measured from falling clock edge after stop bit of read transaction.

QSFP Module Memory Map Description

The QSFP Memory Map, shown in figure 4 below, is used for serial ID, digital monitoring and certain control functions. The memory structure is arranged into a lower, single address space of 128 bytes (0-127) and multiple upper address space pages. The structure permits timely access to address in the lower page such as Interrupt Flags, Monitors, Control and various alarms. The upper memory pages are used for less time critical tasks such as ID information fields, Vendor ID, and

various module and channels thresholds to activate various alarms. The lower page and Upper page 00 is always implemented. Upper page 01 is optional and currently not available. Upper page 02 is optional and implemented. Upper page 03 is implemented.

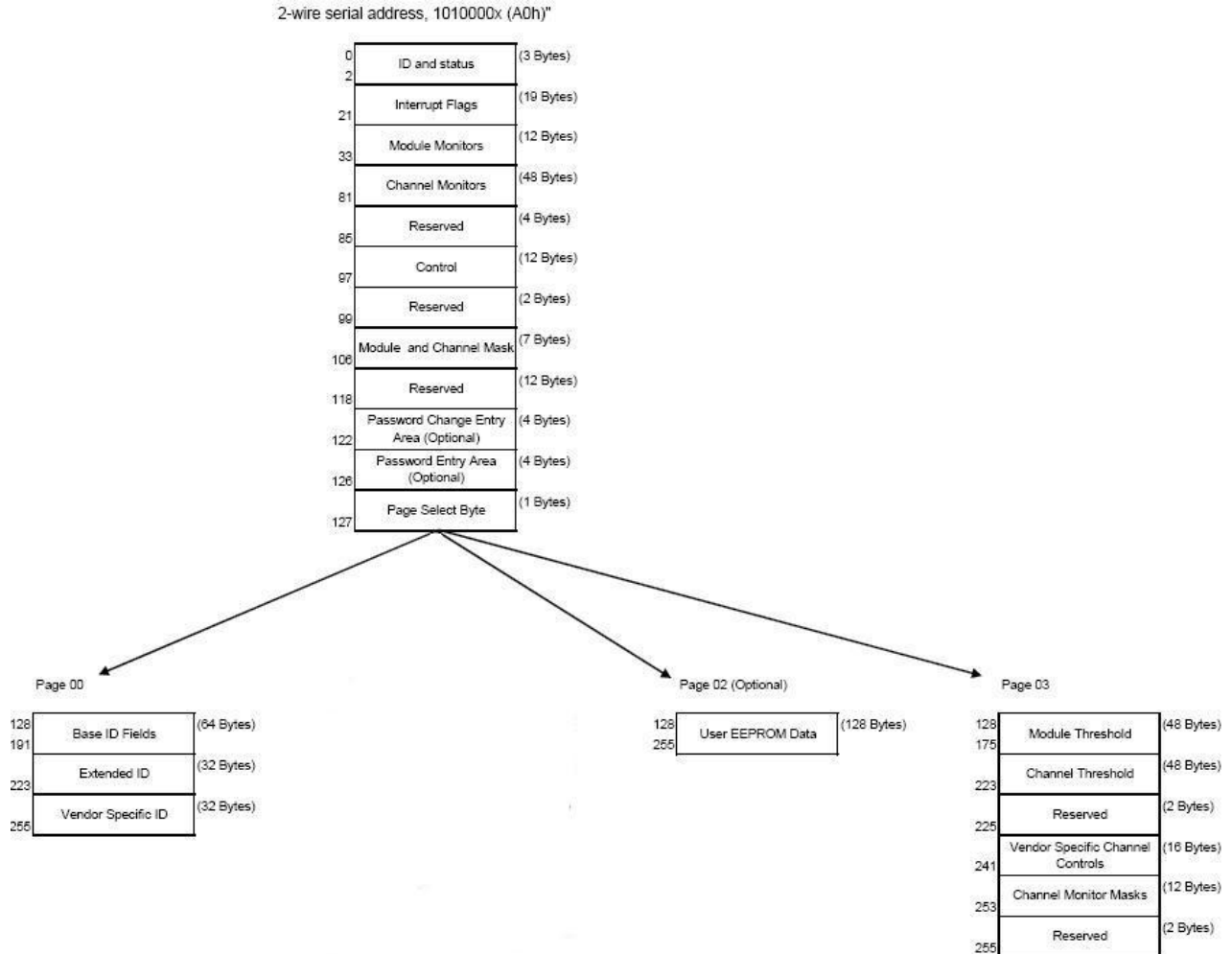


Figure4.QSFP Memory Map

Lower Memory Map Description

The lower 128 bytes of the 2-wire serial bus address space is used to access a variety of measurements and diagnostic functions, a set of control functions, and a means to select which of the various upper memory map pages are accessed on subsequent reads. This portion of the address space is always directly addressable and thus is chosen for monitoring and control

functions that may need to be repeatedly accessed. The definition of Identifier field is the same as page 00h Byte 128.

Lower Memory Map of the QSFP+ module.

| Byte Address | Description | Type |
|--------------|------------------------------------|------------|
| 0 | Identifier(1 Byte) | Read Only |
| 1-2 | Status(2 Bytes) | Read Only |
| 3-21 | Interrupt Flags(19 Bytes) | Read Only |
| 22-33 | Module Monitors(12Bytes) | Read Only |
| 34-81 | Channel Monitors(48 Bytes) | Read Only |
| 82-85 | Reserved (4 Bytes) | Read Only |
| 86-97 | Control(12Bytes) | Read/Write |
| 98-99 | Reserved(2 Bytes) | Read/Write |
| 100-106 | Module and Channel Masks (7 Bytes) | Read/Write |
| 107-126 | Reserved (12 Bytes) | Read/Write |
| 127 | Page Select Byte | Read/Write |

Status Indicator Bits

| Byte | Bit | Name | Description |
|--------------------------|-----|---------------------|---|
| Status Indicators | | | |
| 0 | All | Identifier (1 Byte) | Equal to 0Dh |
| 1 | All | Reserved | |
| 2 | 7 | Reserved | |
| | 6 | Reserved | |
| | 5 | Reserved | |
| | 4 | Reserved | |
| | 3 | Reserved | |
| | 2 | Flat_Mem | Upper memory flat (= '0') or paged ('1'). It set high = '1'. |
| | 1 | IntL | Digital state of the IntL interrupt output pin. |
| | 0 | Data_Not_Ready | Indicates transceiver has not yet achieved power up and monitor data is not ready. Bit remains high until data is ready to be read at which time the device sets the bit low. |

The Data_Not_Ready bit is high during module power up and prior to a valid suite of monitor readings. Once all monitor readings are valid, the bit is set low until the device is powered down.

Channel Status Interrupt Flags

A portion of the memory map (Bytes 3 through 21), form a flag field. Within this field, the status of LOS and Tx Fault as well as alarms and warnings for the various monitored items is reported. In normal conditions, the bits in this field are set to '0'. For the defined conditions of LOS, Tx Fault, module and channel alarms, the appropriate bit or bits are set to '1'.

The **Channel Status Interrupt Flags**, **Module Monitor Interrupt Flags** and **Channel Monitor Interrupt Flags** are defined below.

| Byte | Bit | Name | Description |
|---------------------------------------|-----|----------|-------------------------------------|
| Channel Status Interrupt Flags | | | |
| 3 | 7-4 | Reserved | |
| | 3 | Rx4 LOS | Latched RX LOS indicator, channel 4 |
| | 2 | Rx3 LOS | Latched RX LOS indicator, channel 3 |

| | | | |
|---|-----|-----------|---------------------------------------|
| | 1 | Rx2 LOS | Latched RX LOS indicator, channel 2 |
| | 0 | Rx1 LOS | Latched RX LOS indicator, channel 1 |
| 4 | 7-4 | Reserved | |
| | 3 | Tx4 Fault | Latched TX fault indicator, channel 4 |
| | 2 | Tx3 Fault | Latched TX fault indicator, channel 3 |
| | 1 | Tx2 Fault | Latched TX fault indicator, channel 2 |
| | 0 | Tx1 Fault | Latched TX fault indicator, channel 1 |
| 5 | All | Reserved | |

Notes: A portion of the memory map (Bytes 3 through 21), form a flag field. Within this field, the status of LOS and Tx Fault as well as alarms and warnings for the various monitored items is reported. In normal conditions, the bits in this field are set to '0'. For the defined conditions of LOS, Tx Fault, module and channel alarms, the appropriate bit or bits are set to '1'.

Module Monitor Interrupt Flags

| | | | |
|---|-----|----------------------|-------------------------------------|
| 6 | 7 | L-Temp High Alarm | Latched high temperature alarm |
| | 6 | L- Temp Low Alarm | Latched low temperature alarm |
| | 5 | L- Temp High Warning | Latched high temperature warning |
| | 4 | L- Temp Low Warning | Latched low temperature warning |
| | 3-0 | Reserved | |
| 7 | 7 | L-Vcc High Alarm | Latched high supply voltage alarm |
| | 6 | L-Vcc Low Alarm | Latched low supply voltage alarm |
| | 5 | L-Vcc High Warning | Latched high supply voltage warning |
| | 4 | L-Vcc Low Warning | Latched low supply voltage warning |
| | 3-0 | Reserved | |
| 8 | All | Reserved | |

Channel Monitor Interrupt Flags

| | | | |
|----|---|--------------------------|--|
| 9 | 7 | L-Rx1 Power High Alarm | Latched high RX power alarm, channel 1 |
| | 6 | L-Rx1 Power Low Alarm | Latched low RX power alarm, channel 1 |
| | 5 | L-Rx1 Power High Warning | Latched high RX power warning, channel 1 |
| | 4 | L-Rx1 Power Low Warning | Latched low RX power warning, channel 1 |
| | 3 | L-Rx2 Power High Alarm | Latched high RX power alarm, channel 2 |
| | 2 | L-Rx2 Power Low Alarm | Latched low RX power alarm, channel 2 |
| | 1 | L-Rx2 Power High Warning | Latched high RX power warning, channel 2 |
| | 0 | L-Rx2 Power Low Warning | Latched low RX power warning, channel 2 |
| 10 | 7 | L-Rx3 Power High Alarm | Latched high RX power alarm, channel 3 |
| | 6 | L-Rx3 Power Low Alarm | Latched low RX power alarm, channel 3 |
| | 5 | L-Rx3 Power High Warning | Latched high RX power warning, channel 3 |
| | 4 | L-Rx3 Power Low Warning | Latched low RX power warning, channel 3 |
| | 3 | L-Rx4 Power High Alarm | Latched high RX power alarm, channel 4 |
| | 2 | L-Rx4 Power Low Alarm | Latched low RX power alarm, channel 4 |
| | 1 | L-Rx4 Power High Warning | Latched high RX power warning, channel 4 |
| | 0 | L-Rx4 Power Low Warning | Latched low RX power warning, channel 4 |
| 11 | 7 | L-Tx1 Bias High Alarm | Latched high TX Bias alarm, channel 1 |
| | 6 | L-Tx1 Bias Low Alarm | Latched low TX Bias alarm, channel 1 |
| | 5 | L-Tx1 Bias High Warning | Latched high TX Bias warning, channel 1 |
| | 4 | L-Tx1 Bias Low Warning | Latched low TX Bias warning, channel 1 |
| | 3 | L-Tx2 Bias High Alarm | Latched high TX Bias alarm, channel 2 |
| | 2 | L-Tx2 Bias Low Alarm | Latched low TX Bias alarm, channel 2 |

| | | | |
|-------|-----|--------------------------|--|
| | 1 | L-Tx2 Bias High Warning | Latched high TX Bias warning, channel 2 |
| | 0 | L-Tx2 Bias Low Warning | Latched low TX Bias warning, channel 2 |
| 12 | 7 | L-Tx3 Bias High Alarm | Latched high TX Bias alarm, channel 3 |
| | 6 | L-Tx3 Bias Low Alarm | Latched low TX Bias alarm, channel 3 |
| | 5 | L-Tx3 Bias High Warning | Latched high TX Bias warning, channel 3 |
| | 4 | L-Tx3 Bias Low Warning | Latched low TX Bias warning, channel 3 |
| | 3 | L-Tx4 Bias High Alarm | Latched high TX Bias alarm, channel 4 |
| | 2 | L-Tx4 Bias Low Alarm | Latched low TX Bias alarm, channel 4 |
| | 1 | L-Tx4 Bias High Warning | Latched high TX Bias warning, channel 4 |
| | 0 | L-Tx4 Bias Low Warning | Latched low TX Bias warning, channel 4 |
| 13 | 7 | L-Tx1 Power High Alarm | Latched high TX power alarm, channel 1 |
| | 6 | L-Tx1 Power Low Alarm | Latched low TX power alarm, channel 1 |
| | 5 | L-Tx1 Power High Warning | Latched high TX power warning, channel 1 |
| | 4 | L-Tx1 Power Low Warning | Latched low TX power warning, channel 1 |
| | 3 | L-Tx2 Power High Alarm | Latched high TX power alarm, channel 2 |
| | 2 | L-Tx2 Power Low Alarm | Latched low TX power alarm, channel 2 |
| | 1 | L-Tx2 Power High Warning | Latched high TX power warning, channel 2 |
| | 0 | L-Tx2 Power Low Warning | Latched low TX power warning, channel 2 |
| 14 | 7 | L-Tx3 Power High Alarm | Latched high TX power alarm, channel 3 |
| | 6 | L-Tx3 Power Low Alarm | Latched low TX power alarm, channel 3 |
| | 5 | L-Tx3 Power High Warning | Latched high TX power warning, channel 3 |
| | 4 | L-Tx3 Power Low Warning | Latched low TX power warning, channel 3 |
| | 3 | L-Tx4 Power High Alarm | Latched high TX power alarm, channel 4 |
| | 2 | L-Tx4 Power Low Alarm | Latched low TX power alarm, channel 4 |
| | 1 | L-Tx4 Power High Warning | Latched high TX power warning, channel 4 |
| | 0 | L-Tx4 Power Low Warning | Latched low TX power warning, channel 4 |
| 15-21 | All | Reserved | |

Module Monitoring Values

Module Monitoring Value is intended to measure module temperature and supply voltage. The internally measured Module temperature is represented as a 16-bit signed 2's complement value in increments of 1/256 degrees Celsius as described below. This representation yields a total range of -128°C to $+127^{\circ}\text{C}$. The operational values according to the module specification are considered valid between -10°C and $+85^{\circ}\text{C}$. The module temperature accuracy is better than ± 3 degrees Celsius over the specified operating temperature and voltage.

| | | | | | | | | | | | | | | | |
|------|-------|-------|-------|-------|-------|-------|-------|----------|----------|----------|----------|----------|----------|----------|----------|
| Sign | 2^6 | 2^5 | 2^4 | 2^3 | 2^2 | 2^1 | 2^0 | 2^{-1} | 2^{-2} | 2^{-3} | 2^{-4} | 2^{-5} | 2^{-6} | 2^{-7} | 2^{-8} |
|------|-------|-------|-------|-------|-------|-------|-------|----------|----------|----------|----------|----------|----------|----------|----------|

Temperature word bit weights representation

The internally measured Module supply voltage is represented as a 16-bit unsigned integer with the voltage defined as the full 16 bit value (0 – 65535) with LSB equal to 100 μVolt , yielding a total measurement range of 0 to +6.55 Volts. The accuracy of the voltage is than $\pm 3\%$ of the nominal value over specified operating temperature and voltage.

| Byte | Bit | Name | Description |
|------|-----|------|-------------|
|------|-----|------|-------------|

| Module Monitoring Values | | | |
|--------------------------|-----|--------------------|---|
| 22 | All | Temperature MSB | Internally measured module temperature |
| 23 | All | Temperature LSB | |
| 24-25 | All | Reserved | |
| 26 | All | Supply Voltage MSB | Internally measured module supply voltage |
| 27 | All | Supply Voltage LSB | |
| 28-33 | All | Reserved | |

Channel Monitoring Values

The Channel Monitors for RX Power and TX Bias are defined in the table below:

| Byte | Bit | Name | Description |
|---|-----|-------------------|--|
| Description of Channel Monitor Values (Lower Memory Map) | | | |
| 34 | All | Rx1 power MSB | Internally measured RX input power, channel 1 |
| 35 | All | Rx1 power LSB | |
| 36 | All | Rx2 power MSB | Internally measured RX input power, channel 2 |
| 37 | All | Rx2 power LSB | |
| 38 | All | Rx3 power MSB | Internally measured RX input power, channel 3 |
| 39 | All | Rx3 power LSB | |
| 40 | All | Rx4 power MSB | Internally measured RX input power, channel 4 |
| 41 | All | Rx4 power LSB | |
| 42 | All | Tx1 Bias MSB | Internally measured TX bias, channel 1 |
| 43 | All | Tx1 Bias LSB | |
| 44 | All | Tx2 Bias MSB | Internally measured TX bias, channel 2 |
| 45 | All | Tx2 Bias LSB | |
| 46 | All | Tx3 Bias MSB | Internally measured TX bias, channel 3 |
| 47 | All | Tx3 Bias LSB | |
| 48 | All | Tx4 Bias MSB | Internally measured TX bias, channel 4 |
| 49 | All | Tx4 Bias LSB | |
| 50 | All | Tx1 power MSB | Internally measured TX output power, channel 1 |
| 51 | All | Tx1 power LSB | |
| 52 | All | Tx2 power MSB | Internally measured TX output power, channel 2 |
| 53 | All | Tx2 power LSB | |
| 54 | All | Tx3 power MSB | Internally measured TX output power, channel 3 |
| 55 | All | Tx3 power LSB | |
| 56 | All | Tx4 power MSB | Internally measured TX output power, channel 4 |
| 57 | All | Tx4 power LSB | |
| 58 | All | VCCTX_MONITOR_MSB | |
| 59 | All | VCCTX_MONITOR_LSB | |
| 60 | All | Vcc Rx MSB | Internally measured RX VCC |
| 61 | All | Vcc Rx LSB | |
| 62 | All | VCC1_MONITOR_MSB | |
| 63 | All | VCC1_MONITOR_LSB | |
| 64 | All | TEMP1_MONITOR_MSB | |
| 65 | All | TEMP1_MONITOR_LSB | |
| 66-73 | All | 00h all bytes | Reserved Channel monitor |

The description for the Laser Bias current and Receiver Power Monitors are detailed below.

Laser Bias Current: Measured TX bias current is in mA and are represented as a 16-bit unsigned integer with the current defined as the full 16 bit value (0 – 65535) with LSB equal to 2 uA, yielding a total measurement range of 0 to 131 mA. Accuracy is vendor specific but must be better than $\pm 10\%$ of the manufacturer's nominal value over specified operating temperature and voltage.

Received Power: Measured RX received optical power is in mW and can represent either average received power or OMA depending upon how bit 3 of byte 220 (upper memory page 00h) is set. Represented as a 16 bit unsigned integer with the power defined as the full 16 bit value (0 – 65535) with LSB equal to 0.1 uW, yielding a total measurement range of 0 to 6.5535mW (~-40 to +8.2 dBm). Absolute accuracy is dependent upon the exact optical wavelength. For the vendor specified wavelength, accuracy shall be better than ± 3 dB over specified temperature and voltage. This accuracy shall be maintained for input power levels up to the lesser of maximum transmitted or maximum received optical power per the appropriate standard. It shall be maintained down to the minimum transmitted power minus cable plant loss (insertion loss or passive loss) per the appropriate standard. Absolute accuracy beyond this minimum required received input optical power range is vendor specific.

Control Bytes

There are 4 control bits to enable or disable each of the 4 transmitter channels. Disabling is done by setting any one of the 4 bits of byte 86 to '1'. Bits 0-1 of byte 93 controls the LP Mode functionality of the module. The Control Bytes are described below:

| Byte | Bit | Name | Description |
|--|-----|-----------------|---|
| Description of the Control Bytes. | | | |
| 86 | 7-4 | Reserved | |
| | 3 | Tx4_Disable | Read/write bit that allows software disable of transmitters |
| | 2 | Tx3_Disable | Read/write bit that allows software disable of transmitters |
| | 1 | Tx2_Disable | Read/write bit that allows software disable of transmitters |
| | 0 | Tx1_Disable | Read/write bit that allows software disable of transmitters |
| 87-92 | All | Reserved | All bits are ignored and read as '0's upon power up |
| 93 | 2-7 | Reserved | |
| | 1 | Power_set | Power set to low power mode. Default 0. |
| | 0 | Power_over-ride | Override of LP Mode signal setting the power mode with software |
| 94-99 | | Reserved | |

Module and Channel Masks

The host can control each interrupt event from the QSFP module by masking the corresponding interrupt bits. When a mask bit is written as '1', an interrupt will not occur for this specific event. When the bit is unmasked ('0'), the QSFP will initiate an interrupt by asserting IntL to LOW when a specific event occurs. Using interrupt mask bits enable the host to use polling routine if desirable. The table below depicts the bits and the bytes to mask interrupt events.

| Byte | Bit | Name | Description |
|---|-----|-------------|---|
| Description of Module and channel Interrupt masking bits | | | |
| 86 | 7-4 | Reserved | |
| | 3 | Tx4_Disable | Read/write bit that allows software disable of transmitters |
| | 2 | Tx3_Disable | Read/write bit that allows software disable of transmitters |

| | | | |
|-------|-----|-----------------|--|
| | 1 | Tx2_Disable | Read/write bit that allows software disable of transmitters |
| | 0 | Tx1_Disable | Read/write bit that allows software disable of transmitters |
| 87-92 | All | Reserved | All bits are ignored and read as '0's upon power up |
| 93 | 2-7 | Reserved | |
| | 1 | Power_set | Power set to low power mode. Default 0. |
| | 0 | Power_over-ride | Override of LPMODE signal setting the power mode with software |
| 94-99 | | Reserved | |

Module and Channel Masks

The host can control each interrupt event from the QSFP module by masking the corresponding interrupt bits. When a mask bit is written as '1', an interrupt will not occur for this specific event. When the bit is unmasked ('0'), the QSFP will initiate an interrupt by asserting INTL to LOW when a specific event occurs. Using interrupt mask bits enable the host to use polling routine if desirable. The table below depicts the bits and the bytes to mask interrupt events.

| Byte | Bit | Name | Description |
|---|-----|---------------------|---|
| Description of Module and channel Interrupt masking bits | | | |
| 100 | 7-4 | Reserved | |
| | 3 | M-Rx4 LOS | Masking bit for RX LOS indicator, channel 4 |
| | 2 | M-Rx3 LOS | Masking bit for RX LOS indicator, channel 3 |
| | 1 | M-Rx2 LOS | Masking bit for RX LOS indicator, channel 2 |
| | 0 | M-Rx1 LOS | Masking bit for RX LOS indicator, channel 1 |
| 101 | 7-4 | Reserved | |
| | 3 | M-Tx4 Fault | Masking bit for TX fault indicator, channel 4 |
| | 2 | M-Tx3 Fault | Masking bit for TX fault indicator, channel 3 |
| | 1 | M-Tx2 Fault | Masking bit for TX fault indicator, channel 2 |
| | 0 | M-Tx1 Fault | Masking bit for TX fault indicator, channel 1 |
| 102 | All | Reserved | |
| 103 | 7 | M-Temp High Alarm | Masking bit for high Temperature alarm |
| | 6 | M-Temp Low Alarm | Masking bit for low Temperature alarm |
| | 5 | M-Temp High Warning | Masking bit for high Temperature warning |
| | 4 | M-Temp Low Warning | Masking bit for low Temperature warning |
| | 3-0 | Reserved | |
| 104 | 7 | M-Vcc High Alarm | Masking bit for high Vcc alarm |
| | 6 | M- Vcc Low Alarm | Masking bit for low Vcc alarm |
| | 5 | M- Vcc High Warning | Masking bit for high Vcc warning |
| | 4 | M- Vcc Low Warning | Masking bit for low Vcc warning |
| | 3-0 | Reserved | |
| 105-106 | All | Reserved | |

Password and Page Select

Bytes 119-126 are reserved for an optional password entry function. The Password entry bytes are write only and will be retained until power down, reset, or rewritten by host. This function may be used to control read/write access to vendor specific page 02h. Additionally, module vendors may use this function to implement write protection of Serial ID and other QSFP+ read-only information. Passwords may be supplied to and used by Host manufacturers to limit write access in the User EEPROM Page 02h. Password access shall not be required to access QSFP+ defined data in the lower memory page 00h or in upper pages 00h, 02h and 03h.

Note that multiple module manufacturer passwords may be defined to allow selective access to read or write to various sections of memory as allowed above. Host manufacturer and module manufacturer passwords shall be distinguished by the high order bit (bit 7, byte 123). All host manufacturer passwords shall fall in the range of 00000000h to 7FFFFFFFh, and all module manufacturer passwords in the range of 80000000h to FFFFFFFFh. Host manufacturer passwords shall be initially set to 00001011h in new modules. Host manufacturer passwords may be changed by writing a new password in bytes 119-122 when the correct current Host manufacturer password has been entered in 123-126, with the high order bit being ignored and forced to a value of 0 in the new password. The password entry field shall be set to 00000000h on power up and reset.

| Data Address | Bit | Name of Field | Value | Description of field |
|--------------|-----|---------------------------------------|-------------------------|----------------------|
| 107-118 | All | Reserved | 0000h Read/Write | |
| 119-122 | All | Password Change Entry Area (optional) | 00000000h Read/Write | |
| 123-126 | All | Password Entry Area (optional) | 00000000h Read/Write | |
| 127 | All | Page Select Byte | 00h Read/Write | |

Upper Memory Map Page 00h Description

Page 00h consists of the Serial ID and is used for read only identification information. The Serial ID is divided into the Base_ID Fields, Extended ID Fields and Vendor Specific ID Fields. The format of the Serial ID Memory Map is shown below.

Upper memory map page 00h general description of the QSFP module.

| Address | Size(Bytes) | Name | Description of Base ID Field |
|----------------|-------------|----------------------|---|
| Base_ID Fields | | | |
| 128 | 1 | Identifier | Identifier Type of serial transceiver |
| 129 | 1 | Ext. Identifier | Extended identifier of serial transceiver |
| 130 | 1 | connector | Code for connector type |
| 131-138 | 8 | Transceiver | Code for electronic compatibility or optical compatibility |
| 139 | 1 | Encoding | Code for serial encoding algorithm |
| 140 | 1 | BR,nominal | Nominal bit rate, units of 100 Mbits/s |
| 141 | 1 | Extended Compliance | RateSelect Tags for Extended RateSelect compliance |
| 142 | 1 | Length(SMF) | Link length supported for SMF fiber in km |
| 143 | 1 | Length(E-50um) | Link length supported for EBW 50/125 um fiber, units of 2 m |
| 144 | 1 | Length(50 um) | Link length supported for 50/125 um fiber, units of 1 m |
| 145 | 1 | Length(62.5 um) | Link length supported for 62.5/125 um fiber, units of 1 m |
| 146 | 1 | Length(Copper) | Link length supported for copper, units of 1 m |
| 147 | 1 | Device Tech | Device Technology |
| 148-163 | 16 | Vendor name | QSFP vendor name (ASCII) |
| 164 | 1 | Extended Transceiver | Extended Transceiver Codes for InfiniBand |
| 165-167 | 3 | Vendor OUI | QSFP vendor IEEE company ID |
| 168-183 | 16 | Vendor PN | Part number provided by QSFP vendor (ASCII) |
| 184-185 | 2 | Vendor rev | Revision level for part number provided by vendor (ASCII) |
| 186-187 | 2 | Wavelength | Nominal laser wavelength (wavelength=value/20 in nm) |

| | | | |
|----------------------------------|----|----------------------------|---|
| 188-189 | 2 | Wavelength Tolerance | Guaranteed range of laser wavelength (+/- value) from Nominal wavelength. (wavelength Tol.=value/200 in nm) |
| 190 | 1 | Max Case Temp | Maximum Case Temperature in Degrees C |
| 191 | 1 | CC_BASE | Check code for Base ID Fields(addresses 128-190) |
| Extended ID Fields | | | |
| 192-195 | 4 | Options | Rate Select, TX Disable, TX Fault, LOS |
| 196-211 | 16 | Vendor SN | Serial number provided by vendor (ASCII) |
| 212-219 | 8 | Date code | Vendor's manufacturing date code |
| 220 | 1 | Diagnostic Monitoring Type | Indicates which type of diagnostic monitoring is implemented (if any) in the transceiver. Bit 1, 0 Reserved |
| 221 | 1 | Enhanced Options | Indicates which optional enhanced features are implemented in the transceiver. |
| 222 | 1 | Reserved | Reserved |
| 223 | 1 | CC_EXT | Check code for the Extended ID Fields(addresses 192-222) |
| Vendor Specific ID Fields | | | |
| 224-255 | 32 | Vendor Specific | Vendor Specific EEPROM |

| Byte | Bit | Name of Bit | Description |
|--|----------|---|--|
| Identifier (Address 128) | | | |
| 128 | All | Identifier | 0Dh=QSFP+ |
| Extended Identifier (Address 129) | | | |
| 129 | 7-6 | Ext. Identifier | '11': Power Class 4 Module (3.5 W max. power consumption) |
| | 5 | Reserved | 0 |
| | 4 | NO CLEI code present in Page 02h | 0 |
| | 3 | NO CDR in TX | 0 |
| | 2 | NO CDR in RX | 0 |
| 1-0 | Reserved | 0 | |
| Module Connector Type (Address 130) | | | |
| 130 | All | Connector Type | 07h = LC |
| Transceiver Definition (Address 131-138) | | | |
| 131 | All | Connection Data | 02h = 40GBase-LR 4 |
| 132-138 | All | Reserved | |
| Module Data Encoding (Address 139) | | | |
| 139 | All | Encoding | 00h = unspecified (It is transparent for all givencodes (01h-05h) in the standard. |
| Module Extended Rate and Length (Addresses 140-146) | | | |
| 140-141 | All | Reserved | |
| 142 | All | SMF length support | 0Ah (10km) |
| 143-146 | All | Reserved | |
| Device Technology (Address 147) | | | |
| 147 | 7-4 | Device Technology | 04h = (DFB laser at 1310nm). |
| | 3 | | 0: No wavelength control, 1: Active wavelength control (=0) |
| | 2 | | 0: Uncooled transmitter device, 1: Cooled transmitter (=0) |
| | 1 | | 0: PIN detector, 1: APD detector (=0) |
| 0 | | 0: Transmitter not tunable, 1: Transmitter tunable (=0) | |
| 16 Character Vendor Name (Address 148-163) | | | |
| 148-163 | All | Vendor Name | 'Gigalight' (there are 7 ASCII spaces padded on the right to get 16 characters.) |
| Extended Transceiver Codes (Address 164) | | | |
| 164 | 7-4 | Reserved | |
| | 3 | EDR Speed (20 Gb/s) | 0 |

| | | | |
|--|-----|---|--|
| | 2 | QDR Speed (10 Gb/s) | 1 (support QDR per lane) |
| | 1 | DDR Speed (5.0 Gb/s) | 1 (support DDR per lane) |
| | 0 | SDR Speed (2.5 Gbps) | 1 (support SDR per lane) |
| Vendor Information (Address 165-185) | | | |
| 165-167 | All | Vendor OUI | Organization Unique Identifier |
| 168-183 | All | Vendor PN | GQS-SPO400-LR4CC |
| 184-185 | All | Vendor Rev | Product Revision number |
| Wavelength and Wavelength Tolerance (Address 186-189) | | | |
| 186-189 | | Reserved | |
| Maximum Case Temperature (Address 190) | | | |
| 190 | All | | Standard Temp = 70C = 46h. |
| Check Code Base (Address 191) | | | |
| 191 | All | CC_Base | Low 8 bits of the sum of the content of all page00 byte from 128 to 190 inclusive. |
| Module Options (Address 192-195) | | | |
| 192 | All | | Reserved |
| 193 | 7-1 | | Reserved |
| | 0 | Rx Amplitude Programming | '1' – implemented |
| 194 | 7-4 | Options | Reserved |
| | 3 | Rx_Squelch Disable implemented | '1' – implemented |
| | 2 | Rx_Output Disable capable | '1' – implemented |
| | 1 | Tx Squelch Disable implemented | '0' – Not implemented |
| | 0 | Tx Squelch implemented: | '0' – Not implemented |
| 195 | 7 | Memory page 02 provided | '1' – implemented |
| | 6 | Memory page 01 provided | '0' – Not implemented |
| | 5 | RATE_SELECT is implemented | '0' – Not implemented |
| | 4 | TX_DISABLE is implemented | '1' – implemented |
| | 3 | TX_FAULT signal implemented | '1' – implemented |
| | 2 | Tx Squelch implemented | '0' – Not implemented |
| | 1 | TX Loss of Signal implemented | '0' – Not implemented |
| h | 0 | | Reserved |
| Vendor SN (Address 196-211) | | | |
| 196-211 | All | Vendor SN | yy ww cccc (yy – Year, ww – Work week , cccc – Counter) |
| Module Date Code (Address 212-219) | | | |
| 212-213 | All | Year | Two low order ASCII digits of year (2000=00). |
| 214-215 | All | Month | Two ASCII digits of month (January=01) through (December=12). |
| 216-217 | All | Day | ASCII Code of Day of Month (01-31) |
| 218-219 | All | Lot Code | Vendor Specific Lot number |
| Diagnostic Monitoring Type (Address 220) | | | |
| 220 | 7-4 | Reserved | |
| | 3 | Rx Monitoring is Average Power ('1') or OMA ('0') | '1' |
| | 2-0 | Reserved | |
| Check Code Extended (Address 223) | | | |
| 223 | All | CC_EXT | Low 8 bits of the sum of the content of all page00 byte from 192 to 222 inclusive. |
| Vendor Specific EEPROM (Address 224-255) | | | |
| 224-255 | All | | Vendor Specific Code |

Upper Memory Map Page Description

| Upper Memory Map | Description |
|------------------|-------------|
|------------------|-------------|

| Page | | | |
|------|---|--|------------|
| 01h | Not implemented for user. | | |
| 02h | Page 02 is optionally provided as user writable EEPROM. The host system may read or write this memory for any purpose | | |
| 03h | Byte Address | Description | Type |
| | 128-175 | Module Thresholds(48 Bytes) | Read-Only |
| | 176-223 | Channel Thresholds(48 Bytes) | Read-Only |
| | 224-225 | Reserved(2 Bytes) | Read-Only |
| | 226-239 | Vendor Specific Channel Controls(14 Bytes) | Read/Write |
| | 240-241 | Optional Channel Controls(2 Bytes) | Read/Write |
| | 242-253 | Channel Monitor Masks(12 Bytes) | Read/Write |
| | 254-255 | Reserved(2 Bytes) | Read/Write |

Output Amplitude Control

The output voltage levels of the 4 RX lanes are set using a global register that controls all fourlanes simultaneously. The register definition and default value are given in the table below.

| Output Control per Lane | | | |
|-------------------------|-------------|--------------------------|---------------|
| Byte | Size(Bytes) | Name | Default Value |
| 238 | 3-0 | RX1-RX4 output amplitude | '2'h |

Rx Squelch and Output Disable Control

This enables to control RX_SQ and RX_DIS operation of the transceiver. The default value is '0' upon power up. Therefore Squelch is operational when power up. When '1' is written for specific channel, then this channel Squelch functionality will be disabled. When writing '1' in RX_Output_Disable, the output of this specific channel will be disabled.

| Squelch and Output Disable Controls | | | |
|-------------------------------------|------|--------------------|-------------------------------|
| Byte | Bits | Name | Description |
| 240 | 7 | Rx4_SQ_Disable | Rx Squelch Disable, channel 4 |
| | 6 | Rx3_SQ_Disable | Rx Squelch Disable, channel 3 |
| | 5 | Rx2_SQ_Disable | Rx Squelch Disable, channel 2 |
| | 4 | Rx1_SQ_Disable | Rx Squelch Disable, channel 1 |
| 241 | 7 | Rx4_Output_Disable | Rx Output Disable, channel 4 |
| | 6 | Rx3_Output_Disable | Rx Output Disable, channel 3 |
| | 5 | Rx2_Output_Disable | Rx Output Disable, channel 2 |
| | 4 | Rx1_Output_Disable | Rx Output Disable, channel 1 |
| | 3-0 | Reserved | |

Channel Monitor Masks

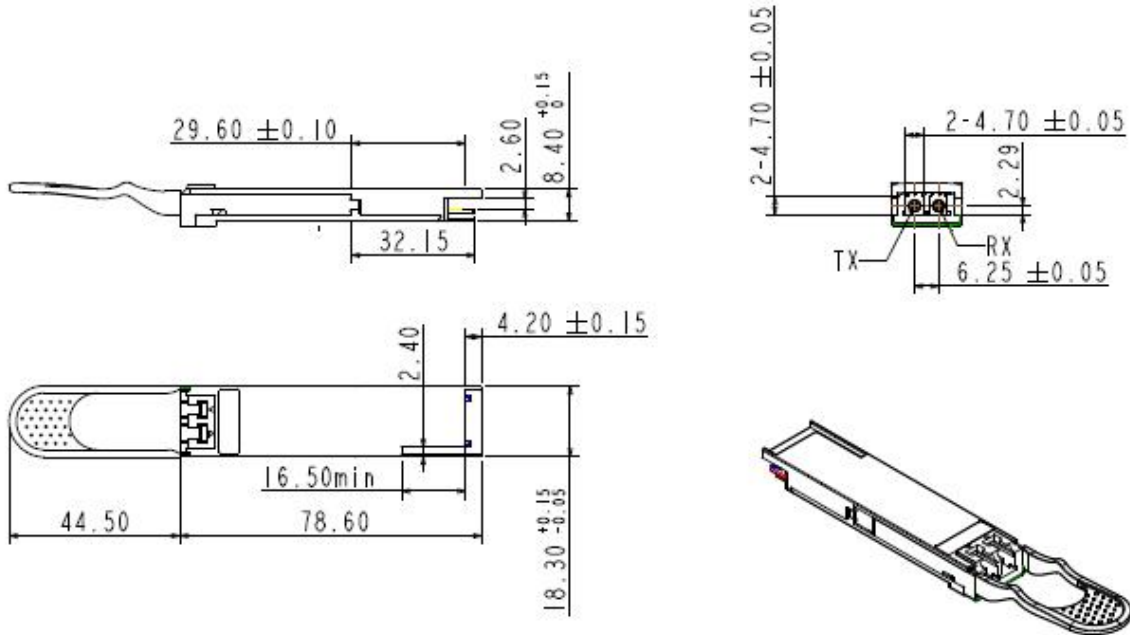
The masking Bits for the Channel Monitor Functions are defined below. When writing '1' in a specific bit location, then this specific channel interrupt is disabled upon reaching specific threshold parameter. The bits can mask High or Low Warning signals or Alarm signals for each individual receiving and transmitting channels.

| Channel Monitor Masks | | | |
|-----------------------|------|--------------------------|--|
| Byte | Bits | Name | Description |
| 242 | 7 | M-Rx1 Power High Alarm | Masking bit for high RX Power alarm, channel 1 |
| | 6 | M-Rx1 Power Low Alarm | Masking bit for low RX Power alarm, channel 1 |
| | 5 | M-Rx1 Power High warning | Masking bit for high RX Power warning, channel 1 |
| | 4 | M-Rx1 Power Low warning | Masking bit for low RX Power warning, channel 1 |
| | 3 | M-Rx2 Power High Alarm | Masking bit for high RX Power alarm, channel 2 |
| | 2 | M-Rx2 Power Low Alarm | Masking bit for low RX Power alarm, channel 2 |

| | | | |
|-----|---|--------------------------|--|
| | 1 | M-Rx2 Power High warning | Masking bit for high RX Power warning, channel 2 |
| | 0 | M-Rx2 Power Low warning | Masking bit for low RX Power warning, channel 2 |
| 243 | 7 | M-Rx3 Power High Alarm | Masking bit for high RX Power alarm, channel 3 |
| | 6 | M-Rx3 Power Low Alarm | Masking bit for low RX Power alarm, channel 3 |
| | 5 | M-Rx3 Power High warning | Masking bit for high RX Power warning, channel 3 |
| | 4 | M-Rx3 Power Low warning | Masking bit for low RX Power warning, channel 3 |
| | 3 | M-Rx4 Power High Alarm | Masking bit for high RX Power alarm, channel 4 |
| | 2 | M-Rx4 Power Low Alarm | Masking bit for low RX Power alarm, channel 4 |
| | 1 | M-Rx4 Power High warning | Masking bit for high RX Power warning, channel 4 |
| | 0 | M-Rx4 Power Low warning | Masking bit for low RX Power warning, channel 4 |
| 244 | 7 | M-Tx1 Bias High Alarm | Masking bit for high TX Bias alarm, channel 1 |
| | 6 | M-Tx1 Bias Low Alarm | Masking bit for low TX Bias alarm, channel 1 |
| | 5 | M-Tx1 Bias High warning | Masking bit for high TX Bias warning, channel 1 |
| | 4 | M-Tx1 Bias Low warning | Masking bit for low TX Bias warning, channel 1 |
| | 3 | M-Tx2 Bias High Alarm | Masking bit for high TX Bias alarm, channel 2 |
| | 2 | M-Tx2 Bias Low Alarm | Masking bit for low TX Bias alarm, channel 2 |
| | 1 | M-Tx2 Bias High warning | Masking bit for high TX Bias warning, channel 2 |
| | 0 | M-Tx2 Bias Low warning | Masking bit for low TX Bias warning, channel 2 |
| 245 | 7 | M-Tx3 Bias High Alarm | Masking bit for high TX Bias alarm, channel 3 |
| | 6 | M-Tx3 Bias Low Alarm | Masking bit for low TX Bias alarm, channel 3 |
| | 5 | M-Tx3 Bias High warning | Masking bit for high TX Bias warning, channel 3 |
| | 4 | M-Tx3 Bias Low warning | Masking bit for low TX Bias warning, channel 3 |
| | 3 | M-Tx4 Bias High Alarm | Masking bit for high TX Bias alarm, channel 4 |
| | 2 | M-Tx4 Bias Low Alarm | Masking bit for low TX Bias alarm, channel 4 |
| | 1 | M-Tx4 Bias High warning | Masking bit for high TX Bias warning, channel 4 |
| | 0 | M-Tx4 Bias Low warning | Masking bit for low TX Bias warning, channel 4 |
| 246 | 7 | M-Tx1 Power High Alarm | Masking bit for high TX Power alarm, channel 1 |
| | 6 | M-Tx1 Power Low Alarm | Masking bit for low TX Power alarm, channel 1 |
| | 5 | M-Tx1 Power High warning | Masking bit for high TX Power warning, channel 1 |
| | 4 | M-Tx1 Power Low warning | Masking bit for low TX Power warning, channel 1 |
| | 3 | M-Tx2 Power High Alarm | Masking bit for high TX Power alarm, channel 2 |
| | 2 | M-Tx2 Power Low Alarm | Masking bit for low TX Power alarm, channel 2 |
| | 1 | M-Tx2 Power High warning | Masking bit for high TX Power warning, channel 2 |
| | 0 | M-Tx2 Power Low warning | Masking bit for low TX Power warning, channel 2 |
| 247 | 7 | M-Tx3 Power High Alarm | Masking bit for high TX Power alarm, channel 3 |
| | 6 | M-Tx3 Power Low Alarm | Masking bit for low TX Power alarm, channel 3 |
| | 5 | M-Tx3 Power High warning | Masking bit for high TX Power warning, channel 3 |
| | 4 | M-Tx3 Power Low warning | Masking bit for low TX Power warning, channel 3 |
| | 3 | M-Tx4 Power High Alarm | Masking bit for high TX Power alarm, channel 4 |
| | 2 | M-Tx4 Power Low Alarm | Masking bit for low TX Power alarm, channel 4 |
| | 1 | M-Tx4 Power High warning | Masking bit for high TX Power warning, channel 4 |

| | | | |
|---------|-----|-------------------------|---|
| | 0 | M-Tx4 Power Low warning | Masking bit for low TX Power warning, channel 4 |
| 248-255 | All | Reserved | |

Mechanical Dimensions



Ordering information

| Part Number | Product Description |
|------------------|---|
| QQS-SPO400-LR4CC | 40Gb/s QSFP+ LR4, Pull-Tab, 10 km on a standard single mode fiber |

ESD

This QSFP LR4 is specified as ESD threshold 1KV for high speed data pins and 2KV for all others electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

Regulatory Compliance

| Feature | Standard |
|--------------------------|---|
| Laser Safety | IEC 60825-1:2014 (Third Edition) |
| Environmental protection | 2011/65/EU |
| CE EMC | EN55032: 2015 EN55024: 2010+A1: 2015 EN61000-3-2:2014 EN61000-3-3:2013 |
| FCC | FCC Part 15, Subpart B; ANSI C63.4-2014 |
| Product Safety | EN/UL 60950-1, 2nd Edition, 2014-10-14 |

Laser Safety

This is a Class 1 Laser Product according to IEC 60825-1:2007. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007).



CAUTION:

Use of controls or adjustment or performance of procedures other than those specified herein may result in hazardous radiation exposure

Important Notice

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