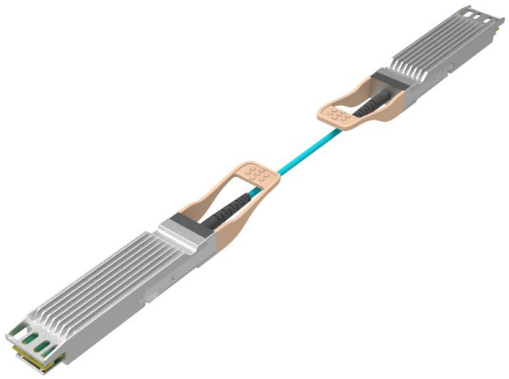
800G OSFP112 AOC Optical Transceiver Module
P/N: GOS-MDO801-XXXC

Features



- ✓ 8 channels full-duplex transceiver modules
- ✓ Transmission data rate up to 106.25G per channel
- ✓ 8x106.25Gbps PAM4 transmitter and PAM4 receiver
- ✓ 8 channels 850nm VCSEL array
- ✓ 8 channels PIN photo detector array
- ✓ Power consumption <14W per end
- ✓ Hot Pluggable OSFP form factor and Compliant with CMIS
- ✓ Maximum link length of 30m on OM3 Multimode Fiber (MMF)and 50m on OM4 MMF with FEC
- ✓ Built-in digital diagnostic functions
- ✓ Operating case temperature 0°C to +70°C
- ✓ 3.3V power supply voltage
- ✓ RoHS compliant(lead free)

Applications

- ✓ IEEE 802.3db 2 x 400GBASE-SR4 Ethernet (PAM4)
- ✓ The transceiver is designed for Ethernet, Telecom and Infiniband use cases.

Description

The Gigalight GOS-MDO801-XXXC is a Eight-Channel, Pluggable, Parallel, Fiber-Optic QSFP Density for 800 Gigabit Ethernet Applications. This transceiver is a high performance module for short-range multi-lane data communication and interconnection applications. It integrates eight data lanes in each direction with 8x53.125GBd. Each lane can operate at 106.25Gbps up to 30 m using OM3 fiber or 50 m using OM4 fiber with FEC. These modules are designed to operate over multimode fiber systems using a nominal wavelength of 850nm. The Common Management Interface Specification (CMIS) for OSFP modules, This module incorporates Gigalight Technologies proven circuit and VCSEL technology to provide reliable long life, high performance, and consistent service.

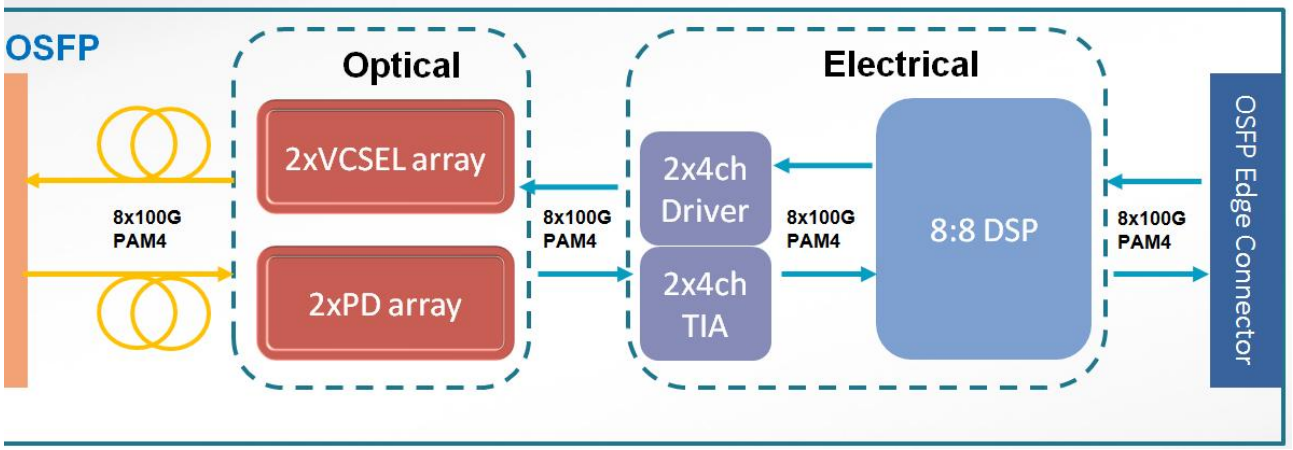


Figure1. Module Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	Vcc	-0.3	3.6	V
Input Voltage	Vin	-0.3	Vcc+0.3	V
Storage Temperature	Tst	-20	85	ºC
Case Operating Temperature	Top	0	70	ºC
Humidity(non-condensing)	Rh	5	95	%

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	Vcc	3.13	3.3	3.47	V
Operating Case temperature	Tca	0		70	ºC
Data Rate Per Lane			106.25		Gbps
Humidity	Rh	5		85	%
Power Dissipation	Pm		13.5	14	W

Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Differential input impedance	Zin	90	100	110	ohm
Differential Output impedance	Zout	90	100	110	ohm
Differential input voltage amplitude	ΔVin	400		900	mVp-p
Differential output voltage	ΔVout			850	mVp-p
Bit Error Rate	BER			2.4E-4	-
Input Logic Level High	V_{IH}	2.0		V_{cc}	V

Input Logic Level Low	V_{IL}	0		0.8	V
Output Logic Level High	V_{OH}	V_{cc}-0.5		V_{cc}	V
Output Logic Level Low	V_{OL}	0		0.4	V
Input Logic Level High	V_{IH}	2.0		V_{cc}	V

Note：

1. BER=2.4E-4; PRBS31Q@53.125GBd. Pre-FEC
2. Differential input voltage amplitude is measured between TxnP and TxnN.
3. Differential output voltage amplitude is measured between RxnP and RxnN.

Optical Characteristics

Table 3 - Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Transmitter						
Centre Wavelength	λc	842	850	948	nm	-
RMS spectral width	Δλ	-	-	0.65	nm	-
Average launch power, each lane	Pout	-4.6	-	5.5	dBm	-
Optical Modulation Amplitude (OMAouter), each lane	OMA	-2.6		4	dBm	-
Transmitter and dispersion eye closure for PAM4(TDECQ),each lane	TDECQ			4.4	dB	
Extinction Ratio	ER	2.5	-	-	dB	-
Average launch power of OFF transmitter, each lane				-30	dB	-
Receiver						
Centre Wavelength	λc	842	850	948	nm	-
Receiver Sensitivity in OMAout	RXsen			max (-4.4,TECQ-6.2)	dBm	1
Stressed Receiver Sensitivity in OMAout	SRS			-1.8	dBm	2

Maximum Average power at receiver , each lane input, each lane				5.5	dBm	-
Minimum Average power at receiver , each lane		-6.3			dBm	
Receiver Reflectance				-15	dB	-
LOS Assert	LOSA	-15		-8.5	dBm	-
LOS De-Assert	LOSD			-6.5	dBm	-
LOS Hysteresis	LOSH	0.5			dB	-

Note：

1. Measured with conformance test signal at TP3 for BER = 2.4E-4 Pre-FEC.
2. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Digital Diagnostic Specification

Parameter	Symbol	Min	Typical	Max	Units	Notes
Transceiver Case Temperature	DMI_Temp	-3		+3	℃	Over operating temp
Supply voltage monitor absolute error	DMI _VCC	-0.1		0.1	V	Full operating range
Channel RX power monitor absolute error	DMI_RX	-2		+2	dB	Per channel
Channel Bias current monitor	DMI_Ibias	-10%		+10%	mA	Per channel
Channel TX power monitor absolute error	DMI_TX	-2		+2	dB	Per channel

Pin Description

Pin	Symbol	Description	Logic	Direction
1	GND	Ground		
2	TX2p	Transmitter Data Non- Inverted	CML-I	Input from Host
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host
4	GND	Ground		
5	TX4p	Transmitter Data Non- Inverted	CML-I	Input from Host
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host
7	GND	Ground		

8	TX6p	Transmitter Data Non- Inverted	CML-I	Input from Host
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host
10	GND	Ground		
11	TX8p	Transmitter Data Non- Inverted	CML-I	Input from Host
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host
13	GND	Ground		
14	SCL	2-wire Serial interface clock	LVCMOS-I/O	Bi- directional
15	VCC	+3.3V Power		Power from Host
16	VCC	+3.3V Power		Power from Host
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	Bi- directional
18	GND	Ground		
19	RX7n	Receiver Data Inverted	CML-O	Output to Host
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host
21	GND	Ground		
22	RX5n	Receiver Data Inverted	CML-O	Output to Host
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host
24	GND	Ground		
25	RX3n	Receiver Data Inverted	CML-O	Output to Host
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host
27	GND	Ground		
28	RX1n	Receiver Data Inverted	CML-O	Output to Host
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host
30	GND	Ground		
31	GND	Ground		
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host
33	RX2n	Receiver Data Inverted	CML-O	Output to Host
34	GND	Ground		
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host
36	RX4n	Receiver Data Inverted	CML-O	Output to Host
37	GND	Ground		
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host
39	RX6n	Receiver Data Inverted	CML-O	Output to Host
40	GND	Ground		
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host
42	RX8n	Receiver Data Inverted	CML-O	Output to Host
43	GND	Ground		
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bi- directional
45	VCC	+3.3V Power		Power from Host

46	VCC	+3.3V Power		Power from Host
47	SDA	2-wire Serial interface data	LVCMOS-I/O	Bi- directional
48	GND	Ground		
49	TX7n	Transmitter Data Inverted	CML-I	Input
50	TX7p	Transmitter Data Non- Inverted	CML-I	Input from Host
51	GND	Ground		
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host
53	TX5p	Transmitter Data Non- Inverted	CML-I	Input from Host
54	GND	Ground		
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host
56	TX3p	Transmitter Data Non- Inverted	CML-I	Input from Host
57	GND	Ground		
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host
59	TX1p	Transmitter Data Non- Inverted	CML-I	Input from Host
60	GND	Ground		

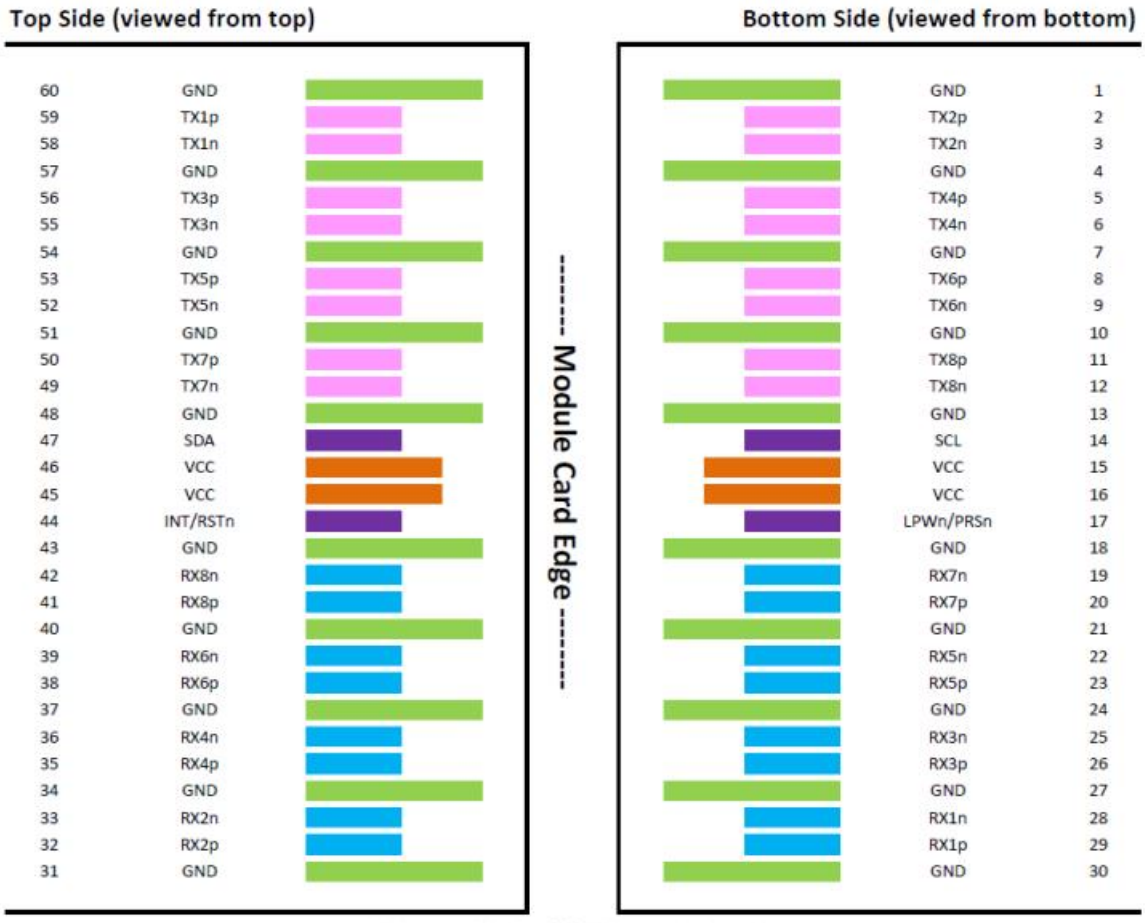


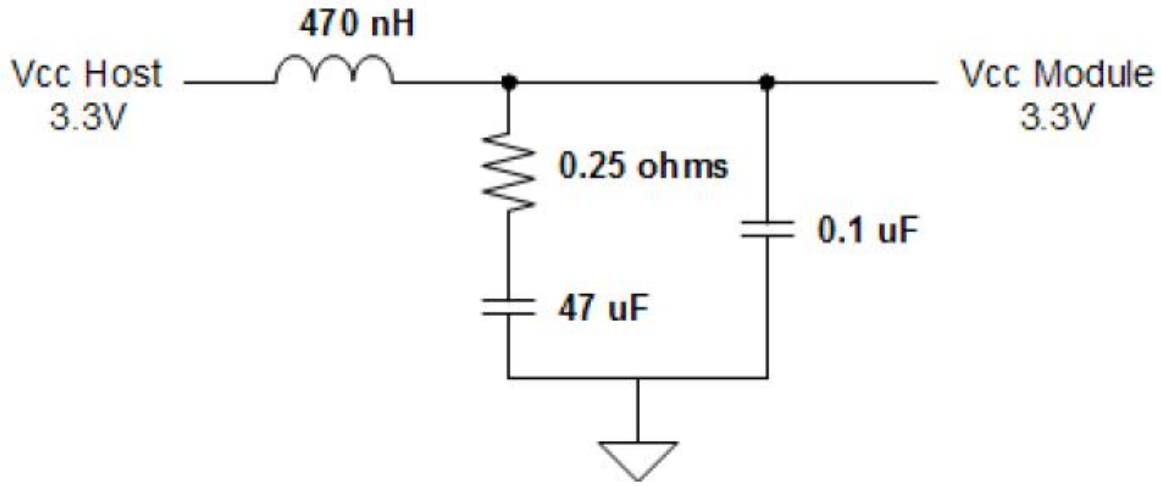
Figure2. Electrical Pin-out Details

OSFP Control pins

Name	Function	Description
LPWn/PRSn	Input/output	Multi-level signal for low power control from host to module and module presence indication from module to host. This signal requires the circuit as described in the OSFP Specification.
INT/RSTn	Input,/output	Multi-level signal for interrupt request from module to host and reset control from host to module. This signal requires the circuit as described in the OSFP Specification.

Name	Function	Description
SCL	BiDir	2-wire serial clock signal. Requires pull-up resistor to 3.3V on host.
SDA	Bidir	2-wire serial data signal. Requires pull-up resistor to 3.3V on host.

Power Supply Filtering



The host board should use the power supply filtering shown in Figure3.

Figure3. Host Board Power Supply Filtering

DIAGNOSTIC MONITORING INTERFACE

Digital diagnostics monitoring function is available on all Gigalight OSFP products. A 2-wire serial interface provides user to contact with module.

Memory Structure and Mapping

This limits the management memory that can be directly accessed by the host to 256 bytes, which is divided in Lower Memory (addresses 00h through 7Fh) and Upper Memory (addresses 80h through

FFh).

A larger addressable management memory is required for all but the most basic modules. This is supported by a structure of 128-byte pages, together with a mechanism for dynamically mapping any of the 128-byte pages from a larger internal management memory space into Upper Memory the host addressable space.

The addressing structure of the additional internal management memory is shown in Figure 4 The management memory inside the module is arranged as a unique and always host accessible address space of 128 bytes (Lower Memory) and as multiple upper address subspaces of 128 bytes each (Pages), only one of which is selected as host visible in Upper Memory. A second level of Page selection is possible for Pages for which several instances exist (e.g. where a bank of pages with the same Page number exists).

This structure supports a flat 256 byte memory for passive copper modules and permits timely access to addresses in the Lower Memory, e.g. Flags and Monitors. Less time critical entries, e.g. serial ID information and threshold settings, are available with the Page Select function in the Lower Page. For more complex modules which require a larger amount of management memory the host needs to use dynamic mapping of the various Pages into the host addressable Upper Memory address space, whenever needed.

Note: The management memory map has been designed largely after the QSFP memory map. This memory map has been changed in order to accommodate 8 electrical lanes and to limit the required memory space. The single address approach is used as found in QSFP. Paging is used in order to enable time critical interactions between host and module.

Supported Pages

A basic 256 byte subset of the Management Memory Map is mandatory for all CMIS compliant devices. Other parts are only available for paged memory modules, or when advertised by the module. See CMIS V4.0 for details regarding the advertisement of supported management memory spaces.

In particular, support of the Lower Memory and of Page 00h is required for all modules, including passive copper cables. These pages are therefore always implemented. Additional support for Pages 01h, 02h and bank 0 of Pages 10h and 11h is required for all paged memory modules.

Bank 0 of pages 10h-1Fh, provides lane-specific registers for the first 8 lanes, and each additional bank provides support for additional 8 lanes. Note, however, that the allocation of information over the banks may be page specific and may not to be related to grouping data for 8 lanes.

The structure allows address space expansion for certain types of modules by allocating additional

Pages. Moreover, additional banks of pages.

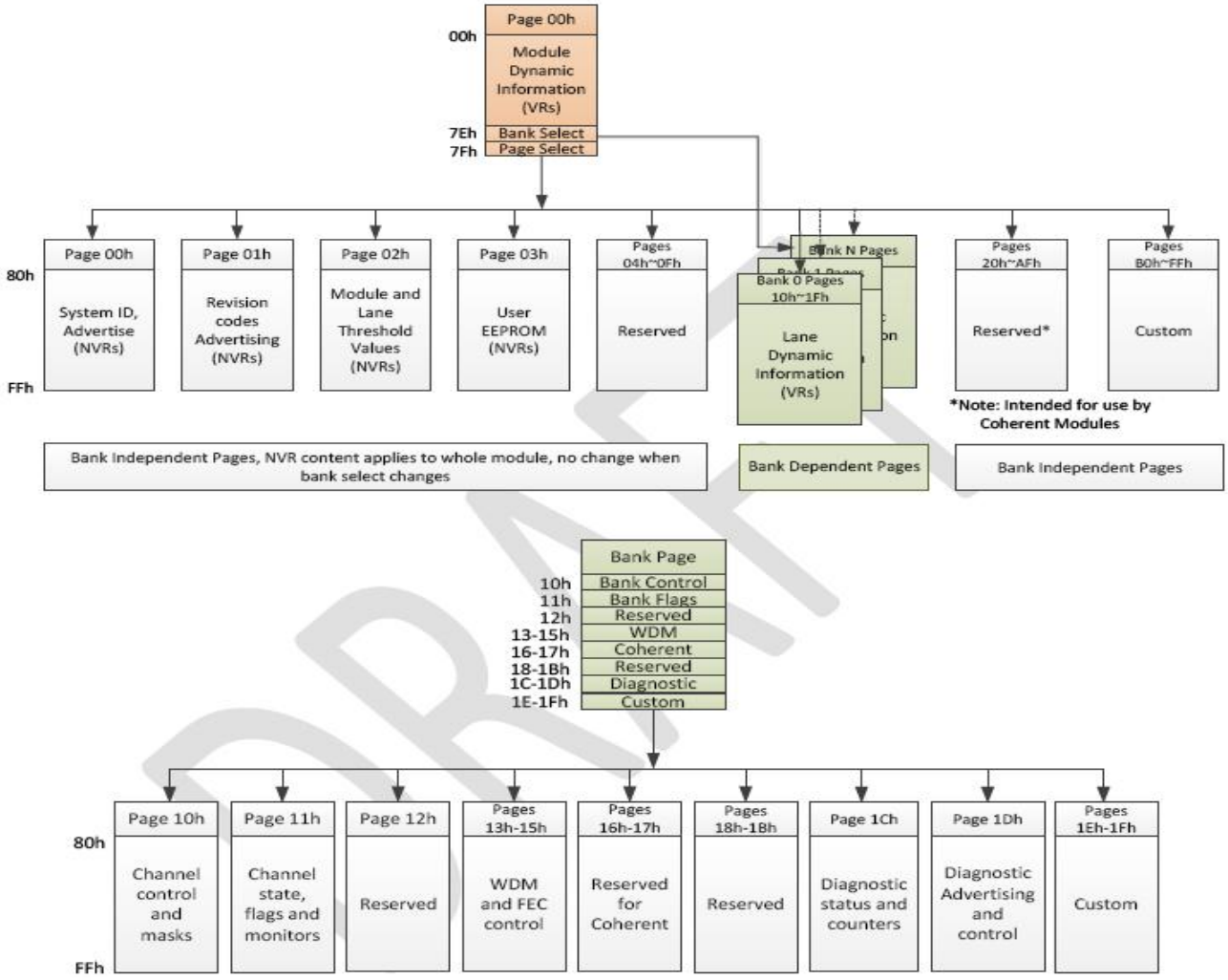


Figure4. OSFP Memory Map

Mechanical Dimensions(mm)

Figure5. Mechanical Specifications

Regulatory Compliance

Gigaligth GOS-MDO801-XXXC transceivers are Class 1 Laser Products. They are certified per the following standards:

Feature	Standard
Laser Safety	IEC 60825-1:2014 (3rd Edition) IEC 60825-2:2004/AMD2:2010 EN 60825-1-2014 EN 60825-2:2004+A1+A2
Electrical Safety	EN 62368-1: 2014 IEC 62368-1:2014 UL 62368-1:2014
Environmental protection	Directive 2011/65/EU with amendment(EU)2015/863
CE EMC	EN55032：2015 EN55035：2017 EN61000-3-2:2014 EN61000-3-3:2013
FCC	FCC Part 15, Subpart B ANSI C63.4-2014

References

1. OSFP_Module_Specification_Rev5_0
2. CMIS V4.0
3. IEEE 802.3db 400GBASE-VR4 Ethernet (PAM4)
4. IEEE802.3ck

⚠CAUTION:

Use of controls or adjustment or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Ordering information

Part Number	Product Description
GOS-MDO801-XXXC	800G OSFP112 AOC transceiver, 850nm, up to 50m with OM4, Finned Top

Important Notice

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Revision History

Revision	Date	Description
V0	Dec-8-2023	Advance Release.