

Optical Interconnection Design Innovator

800G-CR8 (OSFP RHS) Active Copper Cable P/N: GOP-AC801-XXC

Features

- ✓ Hot-plug OSFP RHS form factor
- ✓ Support 8x 100Gb/s PAM4 and NRZ
- ✓ Support up to 5m length
- ✓ 100Ohm differential impedance system
- ✓ 3.3V power supply & typical power consumption 2.5W
- ✓ Commercial case temperature range of 0°C to 70°C
- ✓ I2C management

Applications

- ✓ Infiniband NDR/HDR/EDR
- ✓ Switch / router / HBA
- ✓ Enterprise network
- Data Center Network
- ✓ Data storage and communication industry

STANDARDS COMPLIANCE

- ✓ IEEE P802.3ck D3.0
- ✓ OSFP MSA R4.1
- ✓ CMIS 4.0
- ✓ ROHS

Description

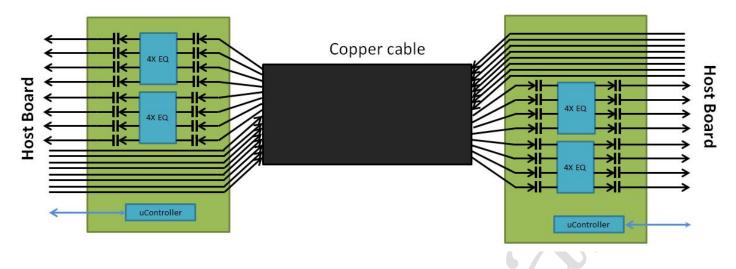
Gigalight's OSFP RHS ACC(Active Copper Cable) assembly series product provide superior signal integrity performance and reliability, comparing to PCC and AOC, ACC is a re-drive solution which built-in linear equalizer to compensate transmission loss, it is an effective solution with low power, low latency, low cost to help high-speed data centers even AI high-computational applications.

 Gigalight's GOP-AC801-XXC cable connects data signals from each of the 16 pairs on the single OSFP RHS end to the other OSFP RHS end, each pair operates at data rates of up to 100Gb/s and can be adaptive downward compatibility. The product operates 3.3V power supply and comply with OSFP MSA and IEEE802.3ck ,it's high performance & cost effective I/O solutions for LAN, HPC and SAN. The high speed cable assemblies meet 400Gigabit Ethernet, Infiniband requirements for performance and reliability.



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Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Storage Temperature	Ts	-20	85	°C
Humidity(non-condensing)	Rh	0	70	°C
Supply Voltage	Vcc	-0.3	3.6	%

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Мах	Unit
Operating Case Temperature	Tc	0		70	°C
Supply Voltage	Vcc	3.13	3.3	3.47	V
Power Consumption	PD		1.3		W
Data Rate per Lane (PAM4)	Fd1		53.125		GBaud/s
Data Rate per Lane (NRZ) Fd2		10.3125	53.125		Gbps
Humidity	Rh	5		85	%

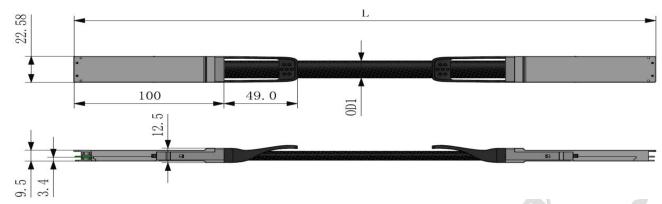


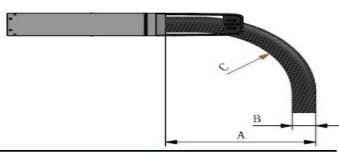
深圳市易飞扬通信技术有限公司 Shenzhen Gigalight Technology Co., Ltd.

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Mechanical Dimensions





OSFP RHS Horizontal Direction				
CABLE GUAGE	DIAMETER"B"	MIN BEND RADIUS"C"	MIN BEND RADIUS"A"	
26AWG	11MM	55MM	65MM	

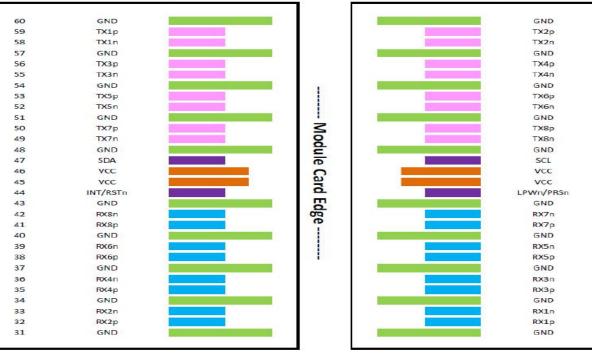
В1
A1

OSFP RHS Vertical Direction					
CABLE GUAGE	DIAMETER"B1"	MIN BEND RADIUS"C1"	MIN BEND RADIUS"A1"		
26AWG	8MM	40MM	50MM		

Bottom Side (viewed from bottom)

Electrical pinout

Top Side (viewed from top)





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Electrical pin list and description

Pin#	Symbol	Description	Logic	Direction	Plug Sequence	Notes
1	GND	Ground			1	
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3	
4	GND	Ground			1	
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3	
7	GND	Ground	Ch (L L	In nut from Linet	1	~
9	TX6p TX6n	Transmitter Data Non-Inverted Transmitter Data Inverted	CML-I CML-I	Input from Host	3	
10	GND	Ground	CIVIL-I	input from Host	1	
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3	
13	GND	Ground	CIVIL I	input iron riost	1	
14	SCL	2-wire Serial interface clock	LVCMOS-I/O	Bi-directional	3	Open-Drain with pull- up resistor on Host
15	VCC	+3.3V Power	1	Power from Host	2	
16	VCC	+3.3V Power		Power from Host	2	
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	Bi-directional	3	See pin description for required circuit
18	GND	Ground			1	
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3	
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
21	GND	Ground			1	
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3	
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
24	GND	Ground			1	
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3	
26	RX3p GND	Receiver Data Non-Inverted Ground	CML-O	Output to Host	3	
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3	
29	RX1p	Receiver Data Inverted	CML-0	Output to Host	3	
30	GND	Ground	CIVIL-O	Output to Host	1	
	OND					
21	GND	Ground				
31	GND RX2p	Ground Receiver Data Non-Inverted	CML-0	Output to Host	1	
31 32 Pin#	GND RX2p Symbol	Ground Receiver Data Non-Inverted Description	CML-O Logic	Output to Host Direction	1 3 Plug	Notes
32 Pin#	RX2p Symbol	Receiver Data Non-Inverted Description	Logic	Direction	1 3 Plug Sequence	Notes
32 Pin# 33	RX2p Symbol RX2n	Receiver Data Non-Inverted Description Receiver Data Inverted			1 3 Plug Sequence 3	Notes
32 Pin# 33 34	RX2p Symbol RX2n GND	Receiver Data Non-Inverted Description Receiver Data Inverted Ground	Logic CML-O	Direction Output to Host	1 3 Plug Sequence 3 1	Notes
32 Pin# 33 34 35	RX2p Symbol RX2n GND RX4p	Receiver Data Non-Inverted Description Receiver Data Inverted Ground Receiver Data Non-Inverted	Logic CML-0 CML-0	Direction Output to Host Output to Host	1 3 Plug Sequence 3 1 3	Notes
32 Pin# 33 34 35 36	RX2p Symbol RX2n GND RX4p RX4n	Receiver Data Non-Inverted Description Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted	Logic CML-O	Direction Output to Host	1 3 Plug Sequence 3 1 3 3 3	Notes
32 Pin# 33 34 35 36 37	RX2p Symbol RX2n GND RX4p RX4n GND	Receiver Data Non-Inverted Description Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground	Logic CML-O CML-O CML-O	Direction Output to Host Output to Host Output to Host	1 3 Plug Sequence 3 1 3 3 1 3 1	Notes
32 Pin# 33 34 35 36 37 38	RX2p Symbol RX2n GND RX4p RX4n GND RX6p	Receiver Data Non-Inverted Description Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted	Logic CML-O CML-O CML-O CML-O	Direction Output to Host Output to Host Output to Host Output to Host	1 3 Plug Sequence 3 1 3 3 1 3 3 3 3	Notes
32 Pin# 33 34 35 36 37 38 39	RX2p Symbol RX2n GND RX4p RX4n GND RX6p RX6n	Receiver Data Non-Inverted Description Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Non-Inverted Receiver Data Inverted	Logic CML-O CML-O CML-O	Direction Output to Host Output to Host Output to Host	1 3 Plug Sequence 3 1 3 3 1 3 3 3 3 3	Notes
32 Pin# 33 34 35 36 37 38 39 40	RX2p Symbol RX2n GND RX4p RX4n GND RX6p RX6n GND	Receiver Data Non-Inverted Description Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Non-Inverted Receiver Data Inverted Ground	Logic CML-O CML-O CML-O CML-O CML-O	Direction Output to Host Output to Host Output to Host Output to Host Output to Host	1 3 Sequence 3 1 3 3 1 3 3 3 1 3 1	Notes
32 Pin# 33 34 35 36 37 38 39 40 41	RX2p Symbol RX2n GND RX4p RX4n GND RX6p RX6p RX6n GND RX8p	Receiver Data Non-Inverted Description Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Inverted Ground Receiver Data Non-Inverted	Logic CML-O CML-O CML-O CML-O CML-O	Direction Output to Host Output to Host Output to Host Output to Host Output to Host Output to Host	1 3 Sequence 3 1 3 3 1 3 3 1 3 3 1 3 3	Notes
32 Pin# 33 34 35 36 37 38 39 40 41 42	RX2p Symbol RX2n GND RX4p RX4n GND RX6p RX6n GND RX6p RX6n GND RX8p RX8p	Receiver Data Non-Inverted Description Receiver Data Inverted Ground Receiver Data Non-Inverted Ground Receiver Data Non-Inverted Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Non-Inverted Receiver Data Non-Inverted Receiver Data Inverted Receiver Data Inverted Receiver Data Inverted Receiver Data Inverted	Logic CML-O CML-O CML-O CML-O CML-O	Direction Output to Host Output to Host Output to Host Output to Host Output to Host	1 3 Plug Sequence 3 1 3 3 1 3 3 1 3 3 3 3 3 3	Notes
32 Pin# 33 34 35 36 37 38 39 40 41	RX2p Symbol RX2n GND RX4p RX4n GND RX6p RX6p RX6n GND RX8p	Receiver Data Non-Inverted Description Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Inverted Ground Receiver Data Non-Inverted	Logic CML-O CML-O CML-O CML-O CML-O	Direction Output to Host Output to Host Output to Host Output to Host Output to Host Output to Host	1 3 Sequence 3 1 3 3 1 3 3 1 3 3 1 3 3	See pin description
32 Pin# 33 34 35 36 37 38 39 40 41 42 43 44	RX2p Symbol RX2n GND RX4p RX4n GND RX6p RX6p RX6n GND RX8p RX8n GND INT/RSTn	Receiver Data Non-Inverted Description Receiver Data Inverted Ground Receiver Data Non-Inverted Ground Receiver Data Inverted Ground Receiver Data Non-Inverted Ground Receiver Data Non-Inverted Ground Receiver Data Non-Inverted Ground Receiver Data Inverted Ground Medule Interrupt / Module Reset	Logic CML-O CML-O CML-O CML-O CML-O CML-O	Direction Output to Host Output to Host Output to Host Output to Host Output to Host Output to Host Output to Host Bi-directional	1 3 Plug Sequence 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 3 1 3	
32 Pin# 33 34 35 36 37 38 39 40 41 42 43 44 45	RX2p Symbol RX2n GND RX4p RX4n GND RX6p RX6n GND RX8p RX8n GND INT/RSTn VCC	Receiver Data Non-Inverted Description Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Non-Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Ground Receiver Data Non-Inverted Has Non-Inverted Receiver Data Non-Invert	Logic CML-O CML-O CML-O CML-O CML-O CML-O	Direction Output to Host Output to Host Output to Host Output to Host Output to Host Output to Host Output to Host Bi-directional Power from Host	1 3 Plug Sequence 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 2	See pin description
32 Pin# 33 34 35 36 37 38 39 40 41 42 43 44 45 46	RX2p Symbol RX2n GND RX4p RX4n GND RX6p RX6n GND RX8p RX8n GND INT/RSTn VCC VCC	Receiver Data Non-Inverted Description Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Non-Inverted Ground Receiver Data Inverted Ground Module Interrupt / Module Reset +3.3V Power +3.3V Power +3.3V Power	Logic CML-O CML-O CML-O CML-O CML-O CML-O Multi-Level	Direction Output to Host Output to Host Output to Host Output to Host Output to Host Output to Host Output to Host Bi-directional Power from Host	1 3 Plug Sequence 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 2 2 2	See pin description for required circuit
32 Pin# 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47	RX2p Symbol RX2n GND RX4p RX4n GND RX6p RX6n GND RX8p RX8n GND INT/RSTn VCC VCC SDA	Receiver Data Non-Inverted Description Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Non-Inverted Ground Module Interrupt / Module Reset +3.3V Power +3.3V Power 2-wire Serial interface data	Logic CML-O CML-O CML-O CML-O CML-O CML-O	Direction Output to Host Output to Host Output to Host Output to Host Output to Host Output to Host Output to Host Bi-directional Power from Host	1 3 Plug Sequence 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 2 2 2 2	See pin description for required circuit
32 9in# 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48	RX2p Symbol RX2n GND RX4p RX4n GND RX6p RX6n GND RX8p RX8n GND INT/RSTn VCC VCC SDA GND	Receiver Data Non-Inverted Description Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Non-Inverted Ground Receiver Data Non-Inverted Ground Receiver Data Non-Inverted Ground Receiver Data Non-Inverted Ground Receiver Data Inverted Ground Module Interrupt / Module Reset +3.3V Power +3.3V Power 2-wire Serial Interface data Ground Ground	Logic CML-O CML-O CML-O CML-O CML-O CML-O CML-O CML-O LVCMOS-I/O	Direction Output to Host Output to Host Bi-directional Power from Host Bi-directional	1 3 Plug 5equence 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 2 2 2 2	See pin description for required circuit
32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49	RX2p Symbol RX2n GND RX4p RX4n GND RX6p RX6n GND RX8p RX8n GND INT/RSTn VCC VCC SDA GND TX7n	Receiver Data Non-Inverted Description Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Non-Inverted Ground Module Interrupt / Module Reset +3.3V Power +3.3V Power 2-wire Serial Interface data Ground Transmitter Data Inverted	Logic CML-O CML-O CML-O CML-O CML-O CML-O Multi-Level	Direction Output to Host Output to Host Bi-directional Power from Host Bi-directional	1 3 Plug 5equence 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 2 2 2 2	See pin description for required circuit
32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50	RX2p Symbol RX2n GND RX4p RX4n GND RX6p RX6p RX6n GND RX8p RX8p RX8p RX8n GND INT/RSTn VCC VCC VCC SDA GND TX7n TX7p	Receiver Data Non-Inverted Description Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Ground Module Interrupt / Module Reset +3.3V Power +3.3V Power 2-wire Serial Interface data Ground Transmitter Data Inverted	Logic CML-O CML-O CML-O CML-O CML-O CML-O CML-O CML-O LVCMOS-I/O	Direction Output to Host Output to Host Bi-directional Power from Host Bi-directional	1 3 Plug 5equence 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 2 2 2 2	See pin description for required circuit
32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51	RX2p Symbol RX2n GND RX4p RX4n GND RX6p RX6p RX6n GND RX8p RX8p RX8n GND INT/RSTn VCC VCC VCC SDA GND TX7n TX7p GND	Receiver Data Non-Inverted Description Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Ground Receiver Data Non-Inverted Ground Receiver Data Non-Inverted Ground Receiver Data Non-Inverted Ground Receiver Data Inverted Ground Module Interrupt / Module Reset +3.3V Power 2-wire Serial Interface data Ground Transmitter Data Inverted Transmitter Data Non-Inverted Ground	Logic CML-O CML-O CML-O CML-O CML-O CML-O Multi-Level LVCMOS-I/O CML-I CML-I	Direction Output to Host Output to Host Output to Host Output to Host Output to Host Output to Host Output to Host Bi-directional Power from Host Bi-directional Input from Host	1 3 Plug 5equence 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 2 2 2 2	See pin description for required circuit
32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50	RX2p Symbol RX2n GND RX4p RX4n GND RX6p RX6p RX6n GND RX8p RX8p RX8p RX8n GND INT/RSTn VCC VCC VCC SDA GND TX7n TX7p	Receiver Data Non-Inverted Description Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Ground Module Interrupt / Module Reset +3.3V Power +3.3V Power 2-wire Serial Interface data Ground Transmitter Data Inverted	Logic CML-O CML-O CML-O CML-O CML-O CML-O Multi-Level	Direction Output to Host Output to Host Bi-directional Power from Host Bi-directional	1 3 Plug 5equence 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 2 2 2 2	See pin description for required circuit
32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51	RX2p Symbol RX2n GND RX4p RX4n GND RX6p RX6p RX6n GND RX8p RX8p RX8n GND INT/RSTn VCC VCC VCC SDA GND TX7n TX7p GND	Receiver Data Non-Inverted Description Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Non-Inverted Ground Receiver Data Inverted Ground Module Interrupt / Module Reset +3.3V Power +3.3V Power 2-wire Serial Interface data Ground Transmitter Data Inverted Transmitter Data Non-Inverted Ground Transmitter Data Inverted Transmitter Data Inverted	Logic CML-O CML-O CML-O CML-O CML-O CML-O Multi-Level LVCMOS-I/O CML-I CML-I	Direction Output to Host Output to Host Output to Host Output to Host Output to Host Output to Host Output to Host Bi-directional Power from Host Bi-directional Input from Host	1 3 Plug Sequence 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 2 2 2 2	See pin description for required circuit
32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52	RX2p Symbol RX2n GND RX4p RX4n GND RX6p RX6p RX6n GND RX8p RX8n GND INT/RSTn VCC VCC VCC SDA GND TX7n TX7p GND TX5n	Receiver Data Non-Inverted Description Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Non-Inverted Ground Receiver Data Inverted Ground Module Interrupt / Module Reset +3.3V Power +3.3V Power 2-wire Serial Interface data Ground Transmitter Data Inverted Transmitter Data Non-Inverted Ground Transmitter Data Inverted Transmitter Data Inverted	Logic CML-0 CML-0 CML-0 CML-0 CML-0 CML-0 Multi-Level LVCMOS-I/0 CML-1 CML-1	Direction Output to Host Bi-directional Power from Host Bi-directional Input from Host Input from Host Input from Host	1 3 Plug Sequence 3 1 3 1 3 1 3 1 3 1 3 1 3 1 3 1 3 1 3 1 3 1 3 1 3 1 3 1 3 1 3 1 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 3 3 3 3 1 3 3 3 3 3 3 3 3 3 3 3 3 3	See pin description for required circuit
32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53	RX2p Symbol RX2n GND RX4p RX4n GND RX6p RX6p RX6n GND RX8p RX8n GND INT/RSTn VCC VCC VCC SDA GND TX7n TX7p GND TX5n TX5p	Receiver Data Non-Inverted Description Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Non-Inverted Ground Receiver Data Inverted Ground Module Interrupt / Module Reset +3.3V Power +3.3V Power 2-wire Serial Interface data Ground Transmitter Data Inverted Transmitter Data Non-Inverted Ground Transmitter Data Inverted Transmitter Data Inverted	Logic CML-0 CML-0 CML-0 CML-0 CML-0 CML-0 Multi-Level LVCMOS-I/0 CML-1 CML-1	Direction Output to Host Bi-directional Power from Host Bi-directional Input from Host Input from Host Input from Host	1 3 Plug Sequence 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 2 2 2 2	See pin description for required circuit
32 Pin# 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54	RX2p Symbol RX2n GND RX4p RX6p RX6p RX8p RX8n GND INT/RSTn VCC VCC SDA GND TX7n TX7p GND TX5n TX5p GND	Receiver Data Non-Inverted Description Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Non-Inverted Ground Receiver Data Inverted Ground Module Interrupt / Module Reset +3.3V Power +3.3V Power 2-wire Serial Interface data Ground Transmitter Data Inverted Transmitter Data Non-Inverted Ground Transmitter Data Non-Inverted Ground Transmitter Data Non-Inverted Ground	Logic CML-O CML-O CML-O CML-O CML-O CML-O Multi-Level LVCMOS-I/O CML-I CML-I CML-I	Direction Output to Host Bi-directional Power from Host Bi-directional Input from Host Input from Hos	1 3 Plug Sequence 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 3 1 3 3 1 3 3 1 3 3 1 3 3 3 1 3 3 1 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 1 3 3 1 1 3 3 1 1 3 3 1 1 3 3 1 1 3 3 1 1 1 1 1 1 1 1 1 1 1 1 1	See pin description for required circuit
32 Pin# 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54	RX2p Symbol RX2n GND RX4p RX6p RX6p RX6n GND RX8p RX8n GND VCC VCC SDA GND TX7n TX7p GND TX5n TX5p GND TX3n	Receiver Data Non-Inverted Description Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Non-Inverted Ground Module Interrupt / Module Reset +3.3V Power +3.3V Power 2-wire Serial Interface data Ground Transmitter Data Inverted Transmitter Data Non-Inverted Ground Transmitter Data Inverted Ground Transmitter Data Inverted Transmitter Data Inverted Transmitter Data Non-Inverted Ground Transmitter Data Inverted Transmitter Data Inverted	Logic CML-O CML-O CML-O CML-O CML-O CML-O CML-O CML-I CML-I CML-I CML-I CML-I CML-I	Direction Output to Host Bi-directional Power from Host Bi-directional Input from Host	1 3 Plug Sequence 3 1 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 3 1 3 3 3 1 3 3 3 3 1 3 3 3 3 3 1 3 3 3 3 3 3 1 3 3 3 3 3 3 3 1 3 3 3 3 3 3 3 3 3 3 3 3 3	See pin description for required circuit
32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56	RX2p Symbol RX2n GND RX4p RX4p RX4n GND RX6p RX6p RX6n GND RX8p RX8n GND INT/RSTn VCC VCC SDA GND TX7n TX7p GND TX7n TX7p GND TX5n TX5p GND TX3n	Receiver Data Non-Inverted Description Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Non-Inverted Ground Module Interrupt / Module Reset +3.3V Power +3.3V Power 2-wire Serial interface data Ground Transmitter Data Inverted Transmitter Data Inverted Ground Transmitter Data Inverted Ground Transmitter Data Non-Inverted Ground Transmitter Data Inverted Transmitter Data Inverted Transmitter Data Non-Inverted Ground Transmitter Data Inverted Transmitter Data Inverted	Logic CML-O CML-O CML-O CML-O CML-O CML-O CML-O CML-I CML-I CML-I CML-I CML-I CML-I	Direction Output to Host Bi-directional Power from Host Bi-directional Input from Host	1 3 Plug Sequence 3 1 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 3 3 3 3 3 3 3 3 3 3	See pin description for required circuit
32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57	RX2pSymbolRX2nGNDRX4pRX4nGNDRX6pRX6nGNDRX8pRX8nGNDINT/RSTnVCCVCCSDAGNDTX7nTX7pGNDTX5pGNDTX3nTX3pGND	Receiver Data Non-Inverted Description Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Non-Inverted Ground Module Interrupt / Module Reset +3.3V Power +3.3V Power 2-wire Serial Interface data Ground Transmitter Data Inverted Transmitter Data Inverted Ground Transmitter Data Inverted Ground Transmitter Data Inverted Transmitter Data Inverted Transmitter Data Inverted Ground Transmitter Data Inverted Ground<	Logic CML-O CML-O CML-O CML-O CML-O CML-O CML-O Multi-Level LVCMOS-I/O CML-I CML-I CML-I CML-I CML-I	Direction Output to Host Bi-directional Power from Host Bi-directional Input from Host Output from Host	1 3 Plug Sequence 3 1 3 1 3 1 3 1 3 1 3 2 2 2 3 1 3 1 3 1 3 1 3 1 3 1 3 1 3 1 3 1 3 1 3 1 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 3 1 3 3 3 3 3 3 3 3 3 3 3 3 3	See pin description for required circuit



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Part Number	GOP-AC801-XXC
Length (meter)	2~5
Wire gauge (AWG)	30/26AWG

If length(meter) is decimal, PN should be as GOP-AC801-DXXC, the wire gauge also can be customized.

Important Notice

Performance figures, data and any illustrative material provided in this data sheet are typical and must be specifically confirmed in writing by Gigalight before they become applicable to any particular order or contract. In accordance with the Gigalight policy of continuous improvement specifications may change without notice.

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Revision History

Revision	Date	Description
Preliminary	May-13-2025	Advance Release.