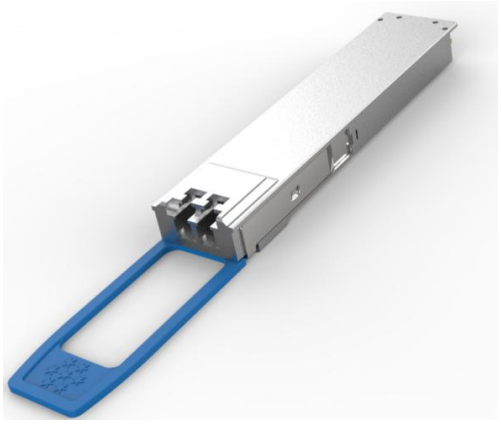
GIGALIGHT 400G OSFP-RHS LR4 10Km EML Transceiver Module

P/N: GOS-SPO401-LR4C

Features



- ✓ 4 channels full-duplex transceiver modules
- ✓ Transmission data rate up to 106.25G per channel
- ✓ 4x106.25Gbps PAM4 transmitter and PAM4 receiver
- ✓ Hot Pluggable OSFP-RHS form factor and Compliant with CMIS
- ✓ Compliant to 400G-LR4 Technical Specification
- ✓ Power consumption <10W
- ✓ Maximum link length of 10Km G.652 SMF with KP-FEC
- ✓ Built-in digital diagnostic functions
- ✓ Operating case temperature 0°C to +70°C
- ✓ 3.3V power supply voltage
- ✓ RoHS compliant(lead free)

Applications

- ✓ 400G-LR4 Technical Spec D2p0
- ✓ CEI-112G-VSR-PAM4
- ✓ OSFP MSA
- ✓ Data center network

Description

This Giglight GOS-SPO401-LR4C product is designed for 10km optical communication applications. The module converts 4 channels of 100Gb/s (PAM4) electrical input data to 4 channels of CWDM optical signals, and multiplexes them into a single channel for 400Gb/s optical transmission. Reversely, on the receiver side, the module optically de-multiplexes a 400Gb/s optical input into 4 channels of CWDM optical signals and converts them to 4 channels of 100Gb/s (PAM4) electrical output data.

The module incorporates 4 independent channels on CWDM4 1271/1291/1311/1331nm center

wavelength, operating at 100G per channel. The transmitter path incorporates 4 independent EML drivers and EML lasers together with an optical multiplexer. On the receiver path, an optical de-multiplexer is coupled to a 4-channel photodiode array.

It is a cost-effective and lower power consumption solution for 400GBASE data center. It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference. The module offers very high functionality and feature integration, accessible via a two-wire serial interface.

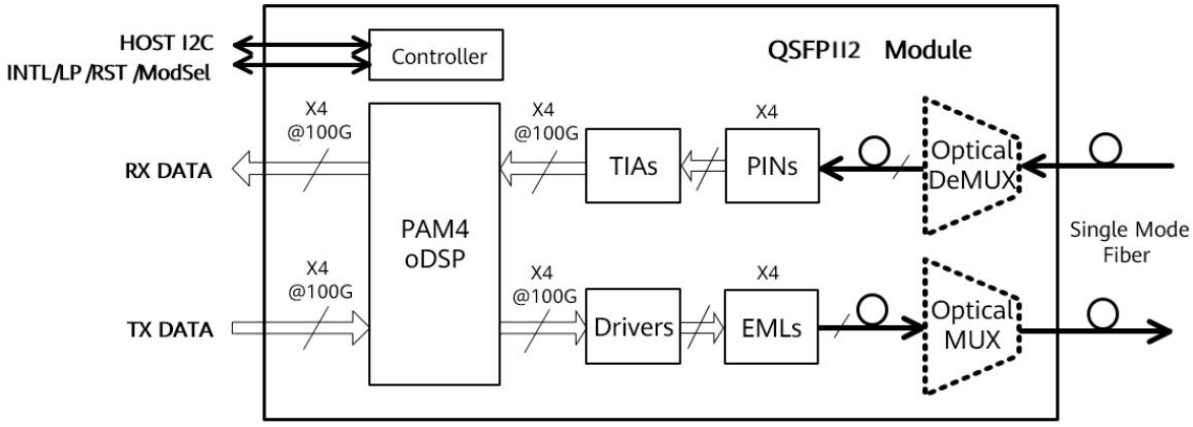


Figure1. Module Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	Vcc	-0.3	3.6	V
Input Voltage	Vin	-0.3	Vcc+0.3	V
Storage Temperature	Tst	-40	85	ºC
Case Operating Temperature	Top	0	70	ºC
Humidity(non-condensing)	Rh	5	95	%

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	Vcc	3.13	3.3	3.47	V
Operating Case temperature	Tca	0		70	ºC
Data Rate Per Lane	fd		106.25		Gbit/s
Humidity	Rh	15		85	%
Power Dissipation	Pm			10	W

Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Differential input impedance	Zin	90	100	110	ohm
Differential Output impedance	Zout	90	100	110	ohm
Differential input voltage amplitude	ΔVin	900			mVp-p
Differential output voltage amplitude	ΔVout			900	mVp-p
Bit Error Rate	BER			2.4E-4	-
Near-end ESMW (Eye symmetry mask width)		0.265			UI
Near-end Eye height, differential (min)		70			mV
Far-end ESMW (Eye symmetry mask width)		0.20			UI
Far-end Eye height, differential (min)		30			mV
Far-end pre-cursor ISI ratio		-4.5		2.5	%

Note：

1) BER=2.4E-4; PRBS31Q@53.125GBd. Pre-FEC
2) Differential input voltage amplitude is measured between TxnP and TxnN.
3) Differential output voltage amplitude is measured between RxnP and RxnN.

Optical Characteristics

Table 3 - Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Transmitter						
Centre Wavelength	λ0	1264.5	1271	1277.5	nm	-
	λ1	1284.5	1291	1297.5	nm	
	λ2	1304.5	1311	1317.5	nm	
	λ3	1324.5	1331	1337.5	nm	
Side-mode suppression ratio	SMSR	30	-	--	dB	-

Average launch power, each lane	Pout	-2.7	-	5.1	dBm	-
Optical Modulation Amplitude(OMA outer), each lane	OMA	0.3	-	4.4	dBm	-
Transmitter and dispersion eye closure for PAM4 (TDECQ),each lane	TDECQ			3.9	dB	
Extinction Ratio	ER	3.5	-	-	dB	-
Average launch power of OFF transmitter, each lane				-16	dB	-
Receiver						
Centre Wavelength	λ0	1264.5	1271	1277.5	nm	-
	λ1	1284.5	1291	1297.5	nm	
	λ2	1304.5	1311	1317.5	nm	
	λ3	1324.5	1331	1337.5	nm	
Receiver Sensitivity in OMA outer	RXsen			-6.8	dBm	1
Average power at receiver , each lane input, each lane	Pin	-9		5.1	dBm	-
Receiver Reflectance				-26	dB	-
LOS Assert		-12			dBm	-
LOS De-Assert				-10	dBm	-
LOS Hysteresis		0.5			dB	-

Note：

1) Measured with conformance test signal at TP3 for BER = 2.4E-4 Pre-FEC

Pin Description

Pin	Logic	Symbol	Name/Description	Plug Sequence[4]	Notes
1		GND	Module Ground	1	1
2	CML-I	Tx2p	Transmitter non-inverted data input	3	
3	CML-I	Tx2n	Transmitter inverted data input	3	
4		GND	Module Ground	1	1
5	CML-I	Tx4p	Transmitter non-inverted data input	3	
6	CML-I	Tx4n	Transmitter inverted data input	3	
7		GND	Module Ground	1	1
8	CML-I	Tx6p	Transmitter non-inverted data input	3	3
9	CML-I	Tx6n	Transmitter inverted data input	3	3
10		GND	Module Ground	1	1
11	CML-I	Tx8p	Transmitter non-inverted data input	3	3
12	CML-I	Tx8n	Transmitter inverted data input	3	3
13		GND	Module Ground	1	1
14	LVCMOS-I/	SCL	2-wire Serial interface clock	3	
15		VCC	+3.3V Power Supply	2	2
16		VCC	+3.3V Power Supply	2	2
17	Multi-Level	LPWn/PRSn	Low-Power Mode / Module Present	3	
18		GND	Module Ground	1	1
19	CML-O	Rx7n	Receiver inverted data output	3	3
20	CML-O	Rx7p	Receiver non-inverted data output	3	3
21		GND	Module Ground	1	1
22	CML-O	Rx5n	Receiver inverted data output	3	3
23	CML-O	Rx5p	Receiver non-inverted data output	3	3
24		GND	Module Ground	1	1
25	CML-O	Rx3n	Receiver inverted data output	3	
26	CML-O	Rx3p	Receiver non-inverted data output	3	
27		GND	Module Ground	1	1
28	CML-O	Rx1n	Receiver inverted data output	3	
29	CML-O	Rx1p	Receiver non-inverted data output	3	
30		GND	Module Ground	1	1
31		GND	Module Ground	1	1

32	CML-O	Rx2p	Receiver non-inverted data output	3	
33	CML-O	Rx2n	Receiver inverted data output	3	
34		GND	Module Ground	1	1
35	CML-O	Rx4p	Receiver non-inverted data output	3	
36	CML-O	Rx4n	Receiver inverted data output	3	
37		GND	Module Ground	1	1
38	CML-O	Rx6p	Receiver non-inverted data output	3	3
39	CML-O	Rx6n	Receiver inverted data output	3	3
40		GND	Module Ground	1	1
41	CML-O	Rx8p	Receiver non-inverted data output	3	3
42	CML-O	Rx8n	Receiver inverted data output	3	3
43		GND	Module Ground	1	1
44	Multi-Level	INT/RSTn	Module Interrupt / Module Reset	3	
45		VCC	+3.3V Power Supply	2	2
46		VCC	+3.3V Power Supply	2	2
47	LVCMOS-I/O	SDA	2-wire Serial interface data	3	
48		GND	Module Ground	1	1
49	CML-I	Tx7n	Transmitter inverted data input	3	3
50	CML-I	Tx7p	Transmitter non-inverted data input	3	3
51		GND	Module Ground	1	1
52	CML-I	Tx5n	Transmitter inverted data input	3	3
53	CML-I	Tx5p	Transmitter non-inverted data input	3	3
54		GND	Module Ground	1	1
55	CML-I	Tx3n	Transmitter inverted data input	3	
56	CML-I	Tx3p	Transmitter non-inverted data input	3	
57		GND	Module Ground	1	1
58	CML-I	Tx1n	Transmitter inverted data input	3	
59	CML-I	Tx1p	Transmitter non-inverted data input	3	
60		GND	Module Ground	1	1

Note：

1): GND is the symbol for signal and supply (power) common for the OSFP-RHS module. All are common within the OSFP-RHS module and all voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

2): VCC are the OSFP-RHS power supplies and shall be applied concurrently. The connector pins are

each rated for a maximum current of 1.5A (max. current of 2.0 A is required for high module power of 15-20W).

3): Not connected in OSFP-RHS.

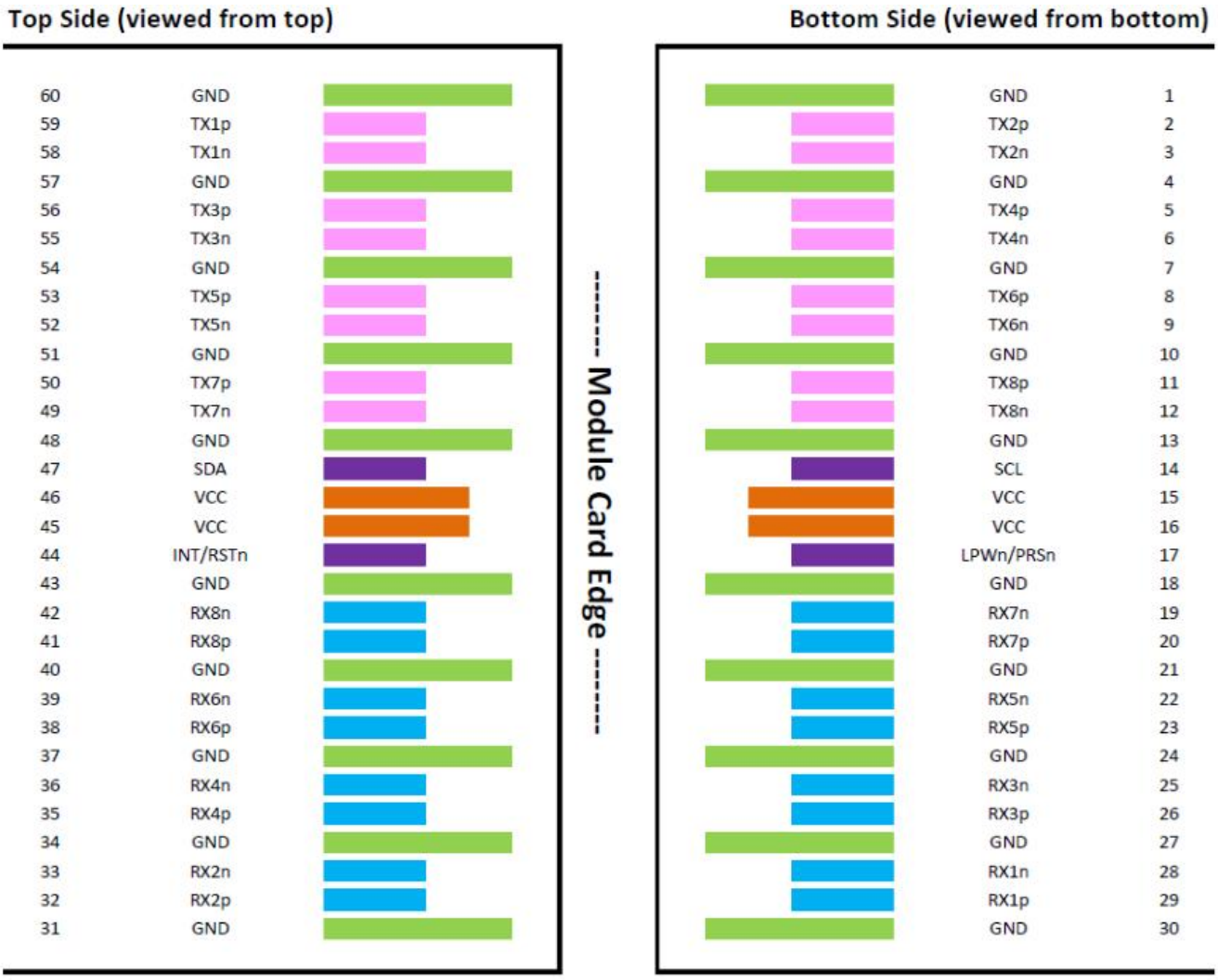


Figure2. OSFP-RHS Module contact assignment

INT/RSTn Pin

INT/RSTn is a dual function signal that allows the module to raise an interrupt to the host, and also allows the host to reset the module. The circuit shown in Figure 3 enables multi-level signaling to provide direct signal control in both directions. Reset is an active-low signal on the host which is translated to an active-low signal on the module. Interrupt is an active-high signal on the module which gets translated to an active-high signal on the host.

The INT/RSTn signal operates in 3 voltage zones to indicate the state of Reset for the module and Interrupt for the host.

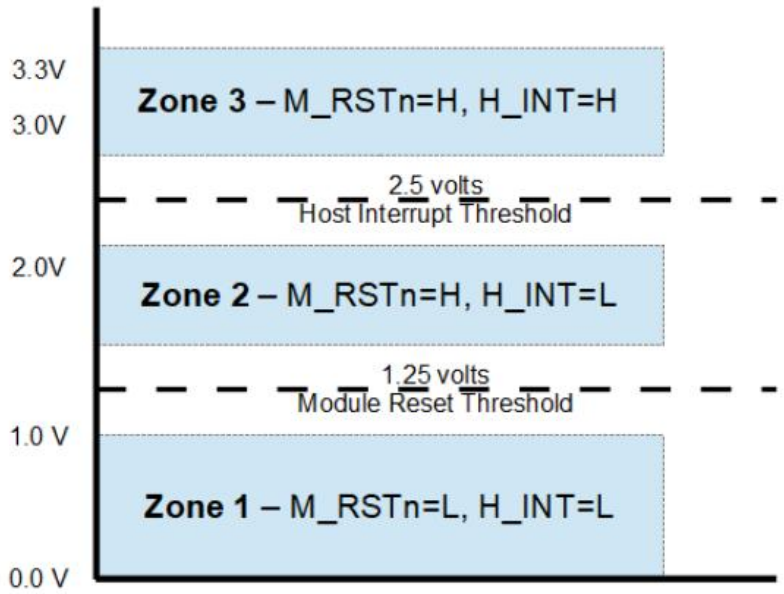


Figure 3. INT/RSTn voltage zones

LPWn/PRSn Pin

LPWn/PRSn is a dual function signal that allows the host to signal Low Power mode and the module to indicate Module Present. The circuit shown in Figure 4 enables multi-level signaling to provide direct signal control in both directions. Low Power mode is an active-low signal on the host which gets converted to an active-low signal on the module. Module Present is controlled by a pull-down resistor on the module which gets converted to an active-low logic signal on the host.

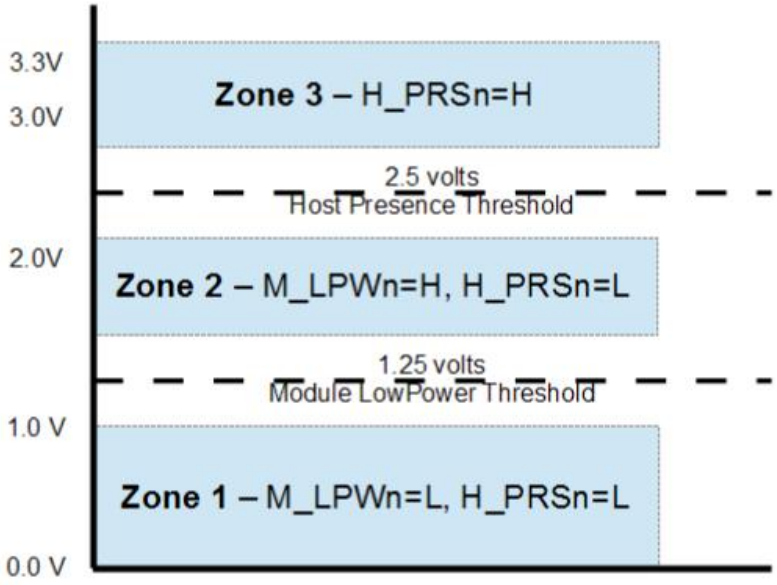


Figure 4. LPWn/PRSn voltage zones

OSFP Host Board and Module Block Diagram

Figure 5 is an example block diagram of the host board's connections to the OSFP module.

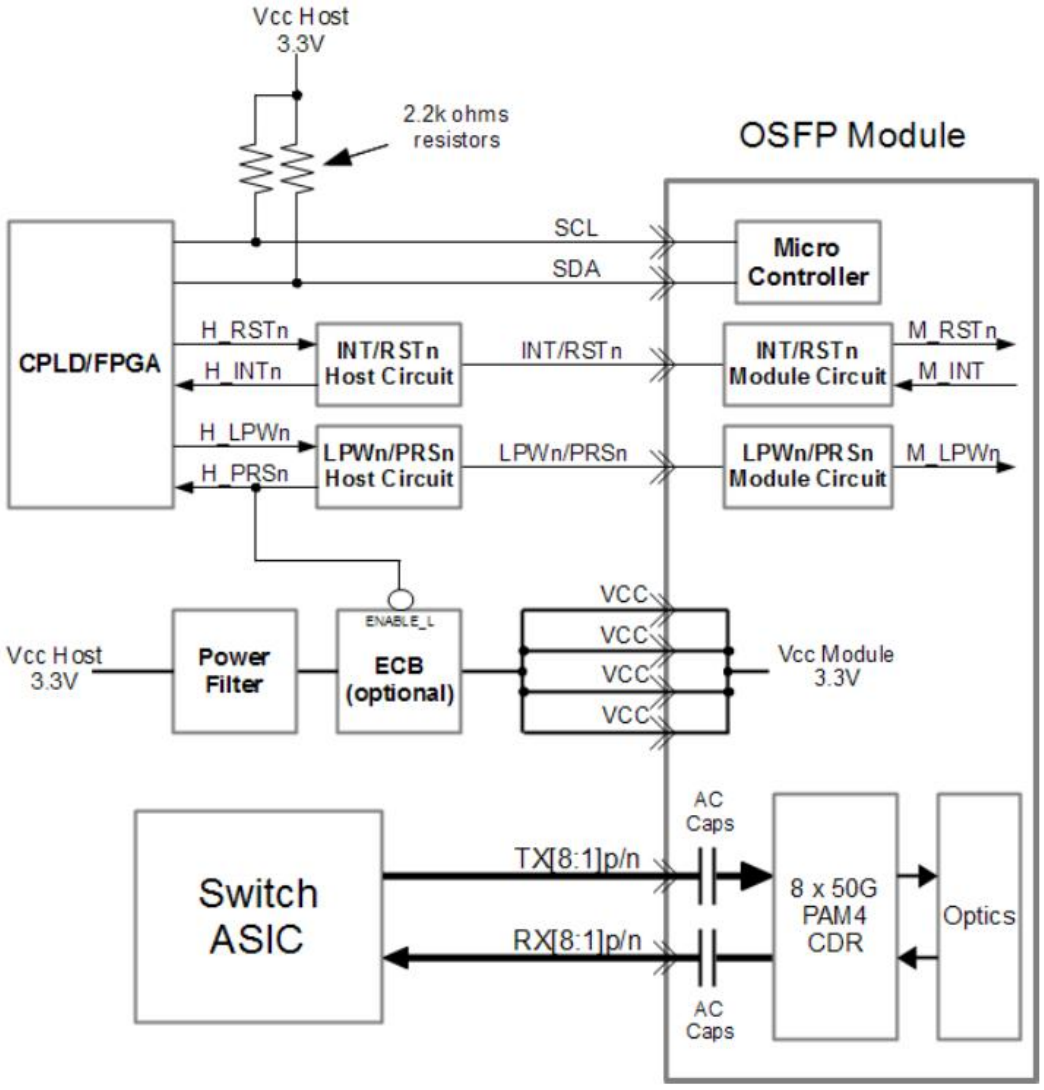


Figure5. Host board and Module block diagram

DIAGNOSTIC MONITORING INTERFACE

Digital diagnostics monitoring function is available on all Gigalight OSFP-RHS products. A 2-wire serial interface provides user to contact with module.

Memory Structure and Mapping

This limits the management memory that can be directly accessed by the host to 256 bytes, which is divided in Lower Memory (addresses 00h through 7Fh) and Upper Memory (addresses 80h through FFh).

A larger addressable management memory is required for all but the most basic modules. This is supported by a structure of 128-byte pages, together with a mechanism for dynamically mapping any of the 128-byte pages from a larger internal management memory space into Upper Memory the host addressable space.

The addressing structure of the additional internal management memory2 is shown in Figure 4 The management memory inside the module is arranged as a unique and always host accessible address space of 128 bytes (Lower Memory) and as multiple upper address subspaces of 128 bytes each (Pages), only one of which is selected as host visible in Upper Memory. A second level of Page selection is possible for Pages for which several instances exist (e.g. where a bank of pages with the same Page number exists).

This structure supports a flat 256 byte memory for passive copper modules and permits timely access to addresses in the Lower Memory, e.g. Flags and Monitors. Less time critical entries, e.g. serial ID information and threshold settings, are available with the Page Select function in the Lower Page. For more complex modules which require a larger amount of management memory the host needs to use dynamic mapping of the various Pages into the host addressable Upper Memory address space, whenever needed.

Note: The management memory map has been designed largely after the QSFP memory map. This memory map has been changed in order to accommodate 8 electrical lanes and to limit the required memory space. The single address approach is used as found in QSFP. Paging is used in order to enable time critical interactions between host and module.

Supported Pages

A basic 256 byte subset of the Management Memory Map is mandatory for all CMIS compliant devices. Other parts are only available for paged memory modules, or when advertised by the module. See CMIS V4.0 for details regarding the advertisement of supported management memory spaces.

In particular, support of the Lower Memory and of Page 00h is required for all modules, including passive copper cables. These pages are therefore always implemented. Additional support for Pages 01h, 02h and bank 0 of Pages 10h and 11h is required for all paged memory modules.

Bank 0 of pages 10h-1Fh, provides lane-specific registers for the first 8 lanes, and each additional bank provides support for additional 8 lanes. Note, however, that the allocation of information over the banks may be page specific and may not to be related to grouping data for 8 lanes.

The structure allows address space expansion for certain types of modules by allocating additional Pages. Moreover, additional banks of pages.

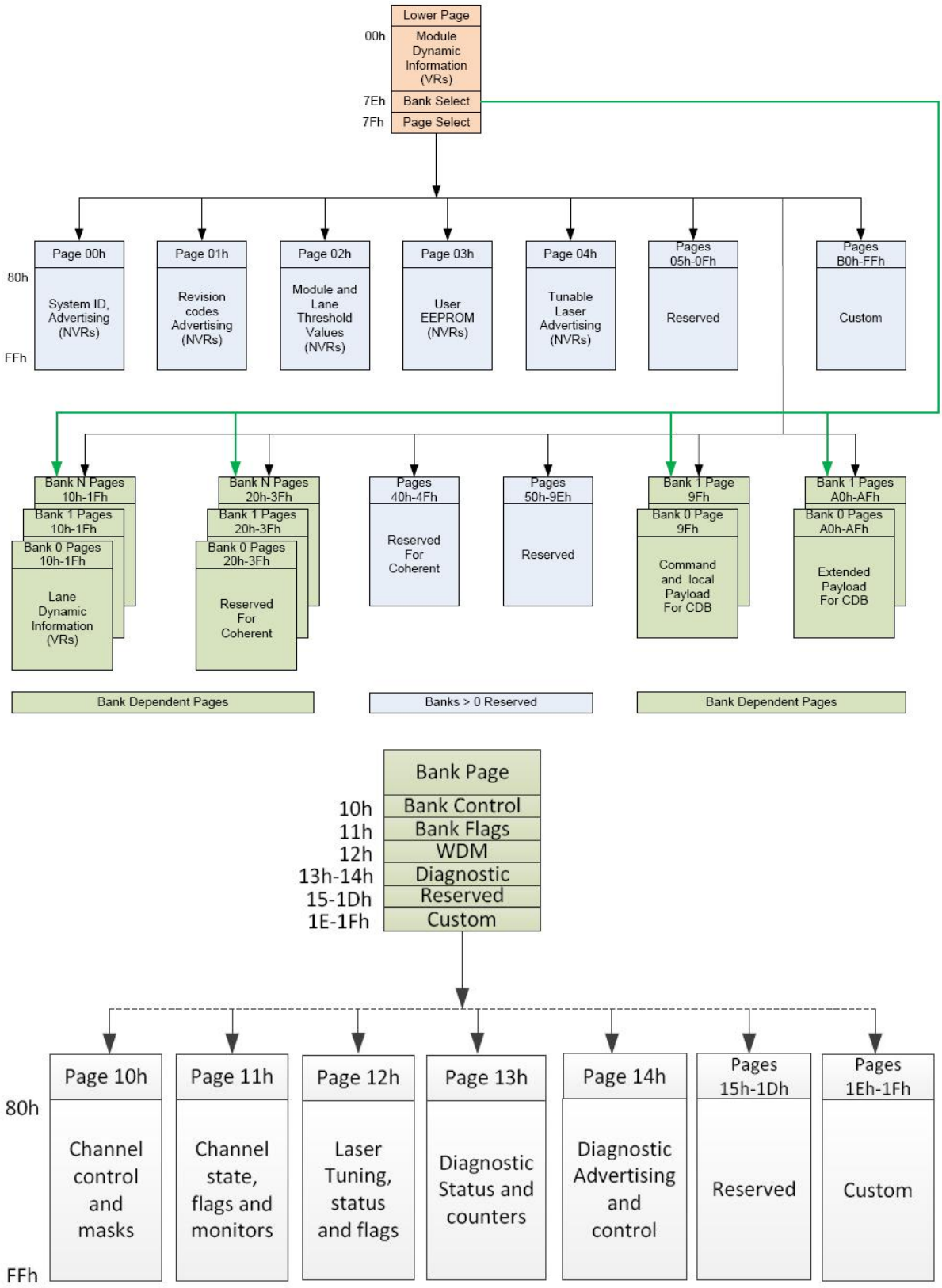


Figure4. QSFP112 Memory Map

Mechanical Dimensions

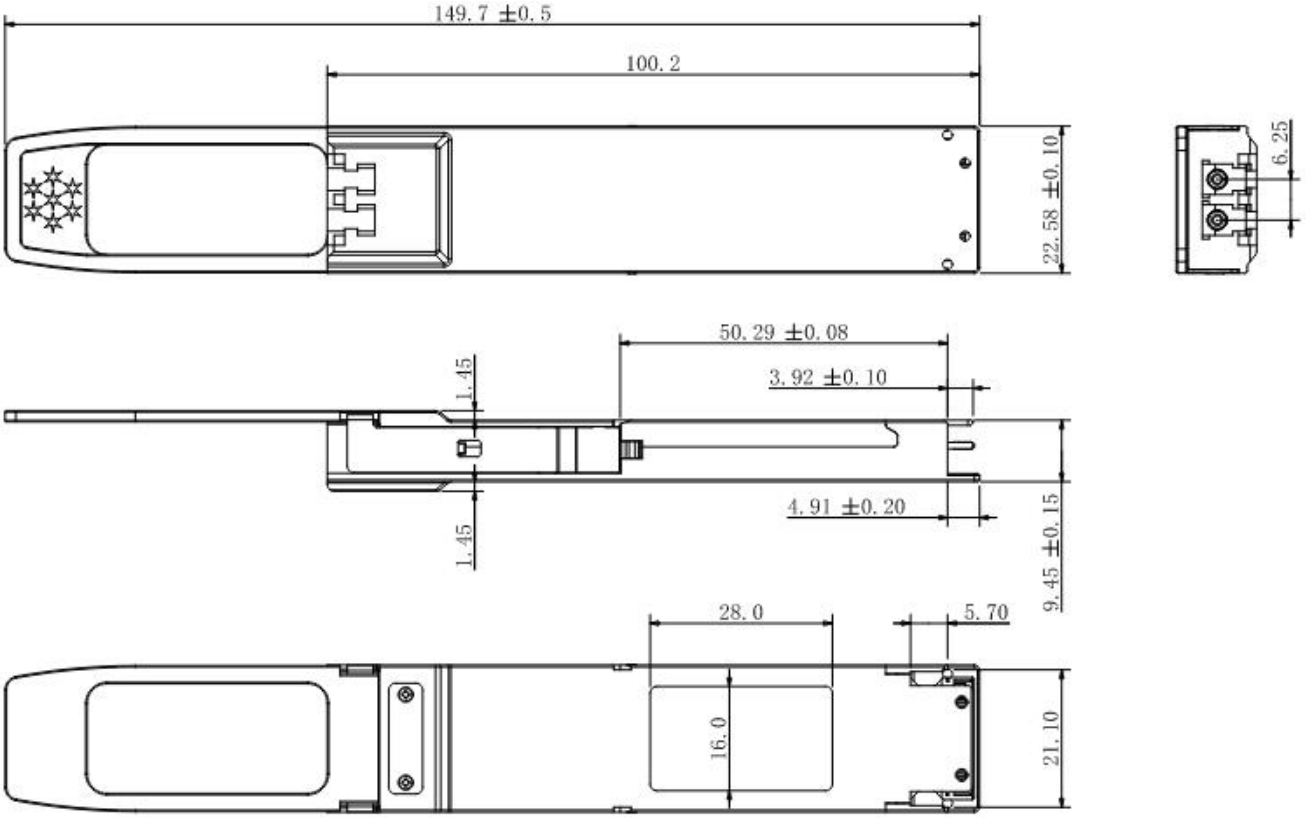


Figure5. Mechanical Specifications

Regulatory Compliance

Gigalight GOS-SPO401-LR4C transceivers are Class 1 Laser Products. They meet the requirements of the following standards：

Feature	Standard
Laser Safety	IEC 60825-1:2014 (3rd Edition) IEC 60825-2:2004/AMD2:2010 EN 60825-1-2014 EN 60825-2:2004+A1+A2
Electrical Safety	EN 62368-1: 2014 IEC 62368-1:2014 UL 62368-1:2014
Environmental protection	Directive 2011/65/EU with amendment(EU)2015/863
CE EMC	EN55032：2015 EN55035：2017 EN61000-3-2:2014 EN61000-3-3:2013

FCC	FCC Part 15, Subpart B ANSI C63.4-2014

References

1. OSFP MSA
2. CMIS 4.0
3. 400G-LR4 Technical Specification
4. IEEE802.3ck
5. OIF CEI-112G-VSR-PAM4

⚠CAUTION:

Use of controls or adjustment or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Ordering information

Part Number	Product Description
GOS-SPO401-LR4C	OSFP-RHS, 400GBASE-LR4, 10Km on Single mode Fiber (SMF),with DSP Power consumption <10W, duplex LC connector.

Important Notice

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Revision History

Revision	Date	Description
V0	Jul-24-2025	Advance Release.