# GIGALIGHT 100G QSFP28 SR Optical Transceiver
P/N: GQS-MPO101-SR1

Features

♦ Full-duplex transceiver modules

♦ 4x25.78125Gbps NRZ electrical interface(CAUI-4)

♦ 106.25Gbps PAM4 transmitter and PAM4 receiver

♦ 850nm VCSEL and PIN receiver

♦ Internal DSP on both receiver and transmitter channels

♦ Power consumption <3.5W

♦ Hot Pluggable QSFP28 form factor

♦ Up to 100m transmission distance on OM4/OM5 MMF with FEC

♦ Duplex LC/APC connector

♦ Built-in digital diagnostic functions

♦ Operating case temperature: 0°C to +70°C

♦ +3.3V power supply

♦ RoHS compliant(lead free)
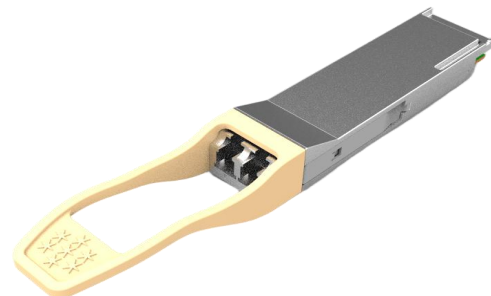
Applications

♦ IEEE 802.3db 100GBASE-SR1

Description

The Gigalight Technologies GQS-MPO101-SR1 is a single-Channel, Pluggable, Fiber-Optic QSFP28 for 106.25Gbps PAM4 Ethernet Applications. It is a high performance module for short-range data communication and interconnect applications which operate at 106.25Gbps up to 100 m using OM4 fiber or 100 m using OM5 fiber. It is compliant with the QSFP28 MSA ,100GBASE-SR1 and CAUI-4(no FEC)1. Digital diagnostics functions are available via the I2C interface, as specified by the QSFP28 MSA.

This module is designed to operate over multimode fiber systems using a nominal wavelength of 850nm.The optical interface uses duplex LC/APC receptacle. This module incorporates Gigalight

Technologies proven circuit and VCSEL technology to provide reliable long life, high performance, and consistent service.

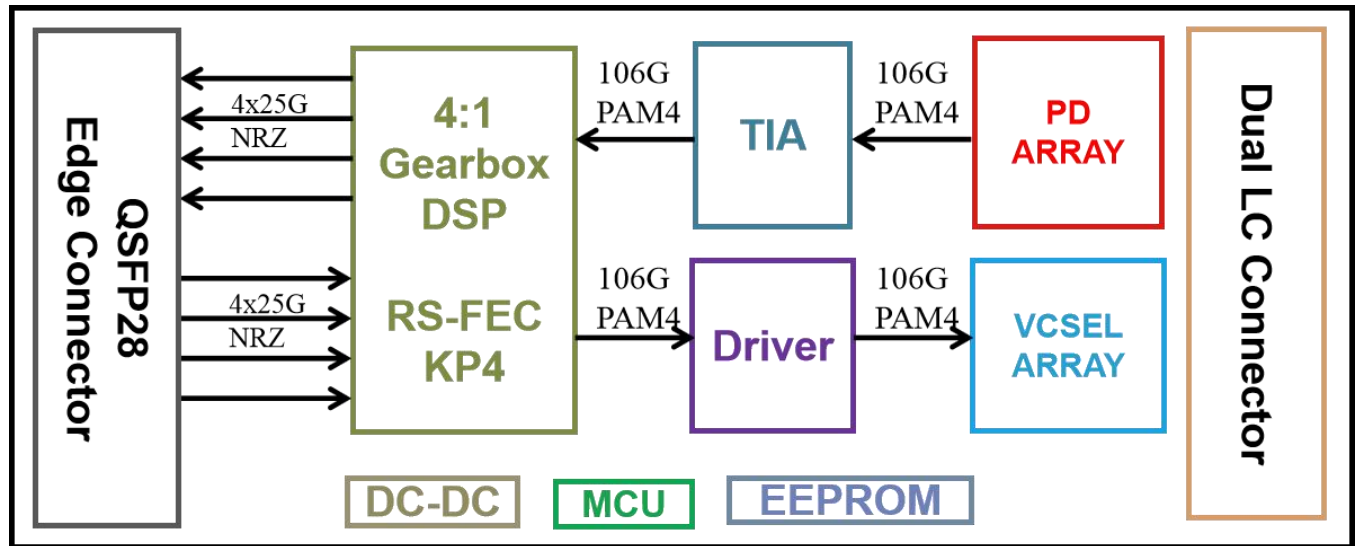1. KR-FEC is optional, please contact us if necessary.

Block Diagram

Figure 1. Module Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage	Vcc	-0.3	3.6	V
Input Voltage	Vin	-0.3	Vcc+0.3	V
Storage Temperature	Tst	-20	85	ºC
Case Operating Temperature	Top	0	70	ºC
Humidity(non-condensing)	Rh	5	95	%

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	V_{cc}	3.13	3.3	3.47	V
Operating Case temperature	T_c	0	-	70	ºC
Data Rate Per Lane	fd	-	106.25	-	Gb/s
Humidity	Rh	5	-	85	%
Power Dissipation	P_m	-	-	3.5	W

Electrical Specifications

Parameter	Symbol	Min.	Typical	Max.	Unit
Differential input impedance	Zin	90	100	110	ohm
Differential Output impedance	Zout	90	100	110	ohm
Differential input voltage Amplitude[1]	ΔVin	400		1600	mVp-p
Differential output voltage Amplitude[2]	ΔVout	-		900	mVp-p
Skew	Sw			300	ps
Bit Error Rate	BER			2.4E-4	-
Input Logic Level High	VIH	2.0		Vcc+0.3	V
Input Logic Level Low	VIL	-0.3		0.8	V
Output Logic Level High	IOH	-50		37.5	uA
Output Logic Level Low	VOL	-0.3		0.4	V
Near-end Eye Linearity		0.85			-

Note：

1. Differential input voltage amplitude is measured between TD+ and TD-.

2. Differential output voltage amplitude is measured between RD+ and RD-.

Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Transmitter						
Centre Wavelength	λc	844	850	863	nm	-
RMS spectral width	Δλ	-	-	0.6	nm	-
Average launch power	Pout	-4.6	-	5	dBm	-
Optical Modulation Amplitude (OMAouter)	OMA	-2.6		3.5	dBm	-
Transmitter and dispersion eye closure for PAM4(TDECQ)	TDECQ			4.4	dB	
Extinction Ratio	ER	2.5	-	-	dB	-

Parameter	Symbol	Min	Typ	Max	Unit	Note
Average launch power of OFF transmitter				-30	dB	-
Receiver						
Centre Wavelength	λc	842	850	948	nm	-
Receiver Sensitivity in OMAout for TECQ≤1.8dB for 1.8＜TECQ≤4.4dB	RXsen			-4.6 -6.4+TECQ	dBm	1
Stressed Receiver Sensitivity in OMAout	SRS			-3.4	dBm	2
Maximum Average power at receiver				5	dBm	-
Minimum Average power at receiver		-6.4			dBm	
Receiver Reflectance				-15	dB	-
LOS Assert	LOSA	-10.5		-8.5	dBm	-
LOS De-Assert – OMA	LOSD			-6.5	dBm	-
LOS Hysteresis	LOSH	0.5			dB	-

Note：

1．Measured with conformance test signal at TP3 for BER = 2.4E-4 Per-FEC

2．These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Diagnostics Specification

Parameter	Range	Unit	Accuracy	Calibration
Temperature	0 to +70	°C	±3°C	Internal / External
Voltage	3.0 to 3.6	V	±3%	Internal / External
Bias Current	0 to 15	mA	±10%	Internal / External
TX Power	-4.6 to +5	dBm	±3dB	Internal / External
RX Power	-6.4 to +5	dBm	±3dB	Internal / External

Digital Diagnostic Monitoring Interface

Digital diagnostics monitoring function is available on all Gigalight QSFP28 transceivers. A 2-wire serial interface provides user to contact with module.

The structure of the memory is shown in Figure 2. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages. This structure permits timely access to addresses in the lower page, such as Interrupt Flags and Monitors. Less time critical time entries, such as serial ID information and threshold settings, are available with the Page Select function.

The interface address used is A0xh and is mainly used for time critical data like interrupt handling in order to enable a one-time-read for all data related to an interrupt situation. After an interrupt, IntL, has been asserted, the host can read out the flag field to determine the affected channel and type of flag.
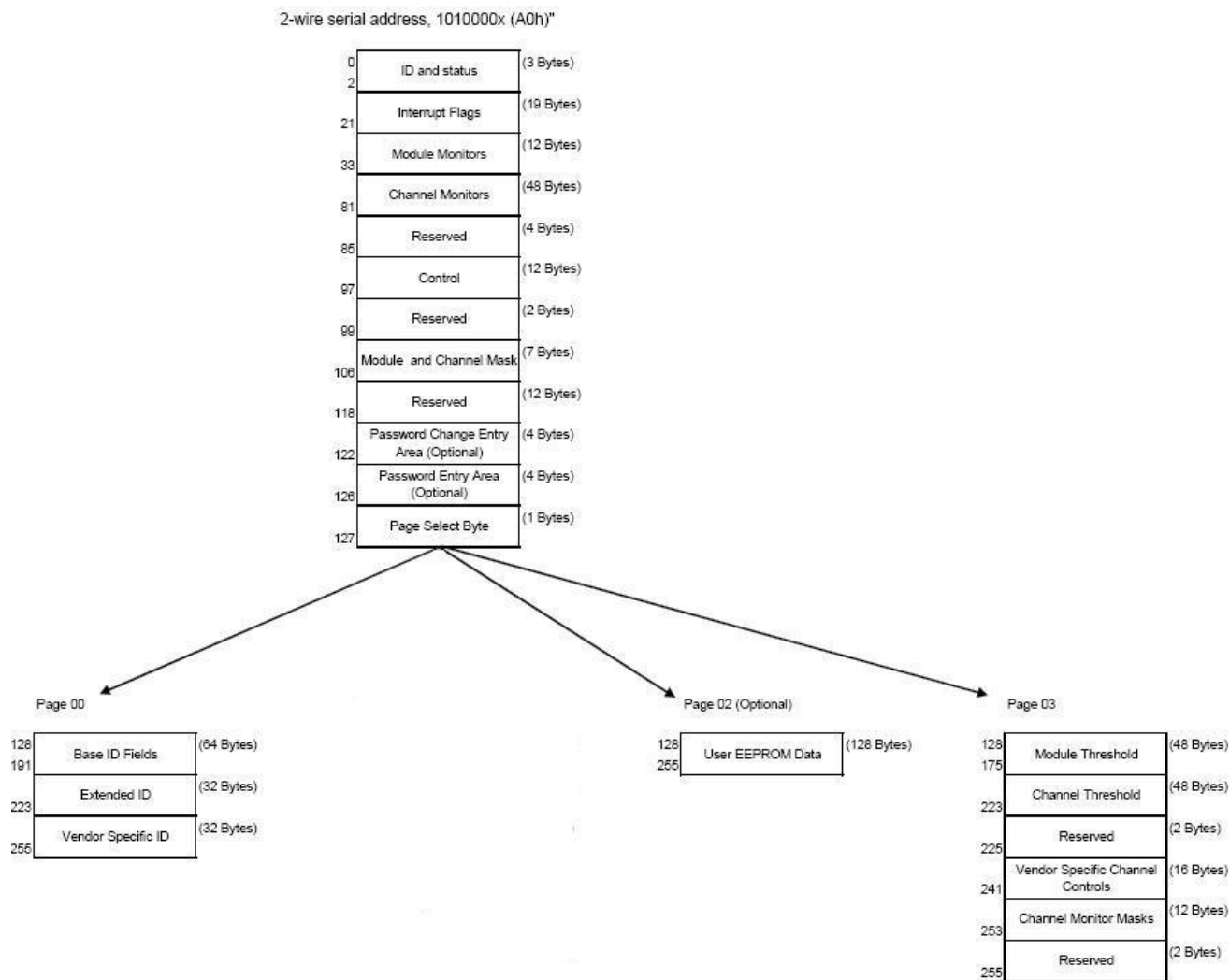
2-wire serial address, 1010000x (A0h)"

Address	Field	Bytes
0–2	ID and status	(3 Bytes)
2–21	Interrupt Flags	(19 Bytes)
21–33	Module Monitors	(12 Bytes)
33–81	Channel Monitors	(48 Bytes)
81–85	Reserved	(4 Bytes)
85–97	Control	(12 Bytes)
97–99	Reserved	(2 Bytes)
99–106	Module and Channel Mask	(7 Bytes)
106–118	Reserved	(12 Bytes)
118–122	Password Change Entry Area (Optional)	(4 Bytes)
122–126	Password Entry Area (Optional)	(4 Bytes)
126–127	Page Select Byte	(1 Bytes)

Page 00

Address	Field	Bytes
128–191	Base ID Fields	(64 Bytes)
191–223	Extended ID	(32 Bytes)
223–255	Vendor Specific ID	(32 Bytes)

Page 02 (Optional)

Address	Field	Bytes
128–255	User EEPROM Data	(128 Bytes)

Page 03

Address	Field	Bytes
128–175	Module Threshold	(48 Bytes)
175–223	Channel Threshold	(48 Bytes)
223–225	Reserved	(2 Bytes)
225–241	Vendor Specific Channel Controls	(16 Bytes)
241–253	Channel Monitor Masks	(12 Bytes)
253–255	Reserved	(2 Bytes)

Figure 2. QSFP28 Memory Map

Byte Address	Description	Type
0	Identifier (1 Byte)	Read Only
1-2	Status (2 Bytes)	Read Only
3-21	Interrupt Flags (31 Bytes)	Read Only
22-33	Module Monitors (12 Bytes)	Read Only
34-81	Channel Monitors (48 Bytes)	Read Only
82-85	Reserved (4 Bytes)	Read Only
86-97	Control (12 Bytes)	Read/Write
98-99	Reserved (2 Bytes)	Read/Write
100-106	Module and Channel Masks (7 Bytes)	Read/Write
107-118	Reserved (12 Bytes)	Read/Write
119-122	Reserved (4 Bytes)	Read/Write
123-126	Reserved (4 Bytes)	Read/Write
127	Page Select Byte	Read/Write

Figure 3. Low Memory Map

Byte Address	Description	Type
128-175	Module Thresholds (48 Bytes)	Read Only
176-223	Reserved (48 Bytes)	Read Only
224-225	Reserved (2 Bytes)	Read Only
226-239	Reserved (14 Bytes)	Read/Write
240-241	Channel Controls (2 Bytes)	Read/Write
242-253	Reserved (12 Bytes)	Read/Write
254-255	Reserved (2 Bytes)	Read/Write

Figure 4. Page 03 Memory Map

Address	Name	Description
128	Identifier (1 Byte)	Identifier Type of serial transceiver
129	Ext. Identifier (1 Byte)	Extended identifier of serial transceiver
130	Connector (1 Byte)	Code for connector type
131-138	Transceiver (8 Bytes)	Code for electronic compatibility or optical compatibility
139	Encoding (1 Byte)	Code for serial encoding algorithm
140	BR, nominal (1 Byte)	Nominal bit rate, units of 100 Mbits/s
141	Extended RateSelect Compliance (1 Byte)	Tags for Extended RateSelect compliance
142	Length SMF (1 Byte)	Link length supported for SM fiber in km
143	Length E-50 μm (1 Byte)	Link length supported for EBW 50/125 μm fiber, units of 2 m
144	Length 50 μm (1 Byte)	Link length supported for 50/125 μm fiber, units of 1 m
145	Length 62.5 μm (1 Byte)	Link length supported for 62.5/125μm fiber, units of 1 m
146	Length copper (1 Byte)	Link length supported for copper, units of 1 m
147	Device Tech (1 Byte)	Device technology
148-163	Vendor name (16 Bytes)	QSFP vendor name (ASCII)
164	Extended Transceiver (1 Byte)	Extended Transceiver Codes for InfiniBand[†]
165-167	Vendor OUI (3 Bytes)	QSFP vendor IEEE vendor company ID
168-183	Vendor PN (16 Bytes)	Part number provided by QSFP vendor (ASCII)
184-185	Vendor rev (2 Bytes)	Revision level for part number provided by vendor (ASCII)
186-187	Wavelength (2 Bytes)	Nominal laser wavelength (Wavelength = value / 20 in nm)
188-189	Wavelength Tolerance (2 Bytes)	Guaranteed range of laser wavelength (+/- value) from Nominal wavelength (Wavelength Tol. = value / 200 in nm)
190	Max Case Temp (1 Byte)	Maximum Case Temperature in Degrees C
191	CC_BASE (1 Byte)	Check code for Base ID fields (addresses 128-190)
192-195	Options (4 Bytes)	Rate Select, TX Disable, TX Fault, LOS
196-211	Vendor SN (16 Bytes)	Serial number provided by vendor (ASCII)
212-219	Date code (8 Bytes)	Vendor's manufacturing date code
220	Diagnostic Monitoring Type (1 Byte)	Indicates which type of diagnostic monitoring is implemented
221	Enhanced Options (1 Byte)	Indicates which optional enhanced features are implemented
222	Reserved (1 Byte)	Reserved
223	CC_EXT	Check code for the Extended ID Fields (addresses 192-222)
224-255	Vendor Specific (32 Bytes)	Vendor Specific EEPROM

Figure 5. Page 00 Memory Map

Page02 is User EEPROM and its format decided by user.

The detail description of low memory and Page 00, Page 03 upper memory please see SFF-8436
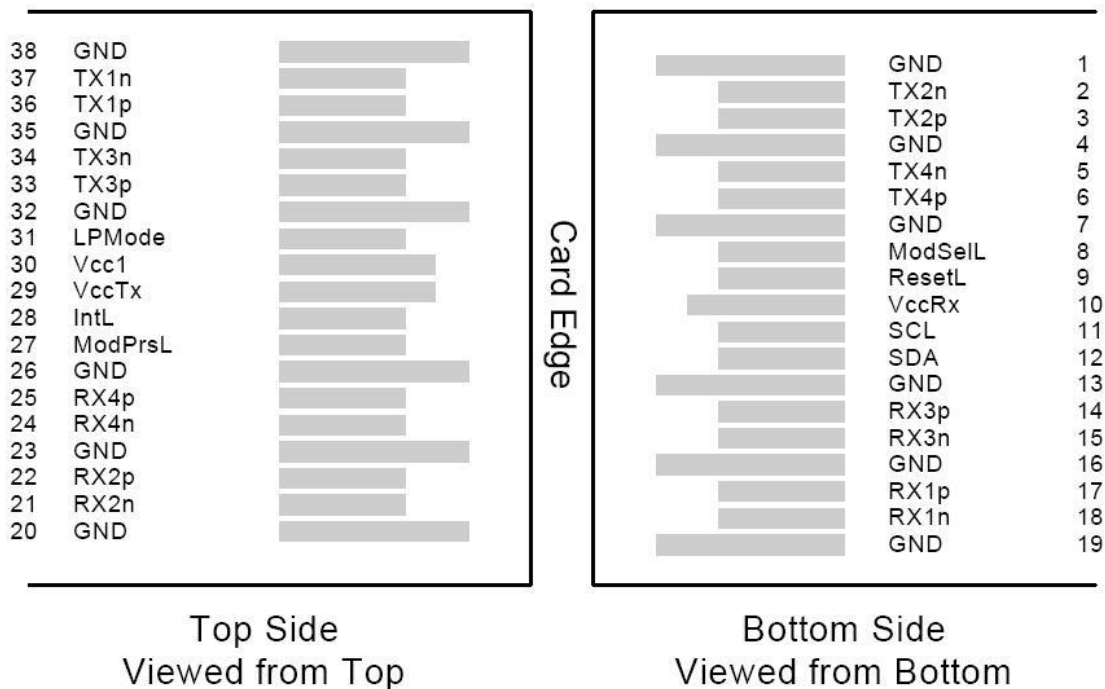
document.

Pin Definitions

Figure 6. Pin View

Pin Description

Pin	Logic	Symbol	Name/Description
1		GND	Module Ground[1]
2	CML-I	Tx2-	Transmitter inverted data input
3	CML-I	Tx2+	Transmitter non-inverted data input
4		GND	Module Ground[1]
5	CML-I	Tx4-	Transmitter inverted data input
6	CML-I	Tx4+	Transmitter non-inverted data input
7		GND	Module Ground[1]
8	LVTTL-I	MODSEIL	Module Select[2]
9	LVTTL-I	ResetL	Module Reset[2]
10		VCCRx	+3.3V Receiver Power Supply
11	LVCMOS-I	SCL	2-wire Serial interface clock[2]
12	LVCMOS-I/O	SDA	2-wire Serial interface data[2]
13		GND	Module Ground[1]
14	CML-O	RX3+	Receiver non-inverted data output
15	CML-O	RX3-	Receiver inverted data output

16		GND	Module Ground[1]
17	CML-O	RX1+	Receiver non-inverted data output
18	CML-O	RX1-	Receiver inverted data output
19		GND	Module Ground[1]
20		GND	Module Ground[1]
21	CML-O	RX2-	Receiver inverted data output
22	CML-O	RX2+	Receiver non-inverted data output
23		GND	Module Ground[1]
24	CML-O	RX4-	Receiver inverted data output
25	CML-O	RX4+	Receiver non-inverted data output
26		GND	Module Ground[1]
27	LVTTL-O	ModPrsL	Module Present, internal pulled down to GND
28	LVTTL-O	IntL	Interrupt output, should be pulled up on host board[2]
29		VCCTx	+3.3V Transmitter Power Supply
30		VCC1	+3.3V Power Supply
31	LVTTL-I	LPMode	Low Power Mode[2]
32		GND	Module Ground[1]
33	CML-I	Tx3+	Transmitter non-inverted data input
34	CML-I	Tx3-	Transmitter inverted data input
35		GND	Module Ground[1]
36	CML-I	Tx1+	Transmitter non-inverted data input
37	CML-I	Tx1-	Transmitter inverted data input
38		GND	Module Ground[1]

Note:

1. Module circuit ground is isolated from module chassis ground within the module.

2. Open collector should be pulled up with 4.7K to 10K ohms on host board to a voltage between 3.15V and 3.6V.

ModSelL Pin

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP modules on a single 2-wire interface bus. When the ModSelL is "High", the module will not respond to any 2-wire interface communication from the host. ModSelL has an internal pull-up in the module.

ResetL Pin

Reset. LPMode_Reset has an internal pull-up in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module will post this completion of reset interrupt without requiring a reset.

LPMode Pin

Gigalight QSFP28 modules operate in the low power mode (less than 1.5 W power consumption). This pin active high will decrease power consumption to less than 1W.

ModPrsL Pin

ModPrsL is pulled up to Vcc on the host board and grounded in the module. The ModPrsL is asserted "Low" when the module is inserted and deasserted "High" when the module is physically absent from the host connector.

IntL Pin

IntL is an output pin. When "Low" , it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt by using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled up to Vcc on the host board.

Power Supply Filtering

The host board should use the power supply filtering shown in Figure 7.
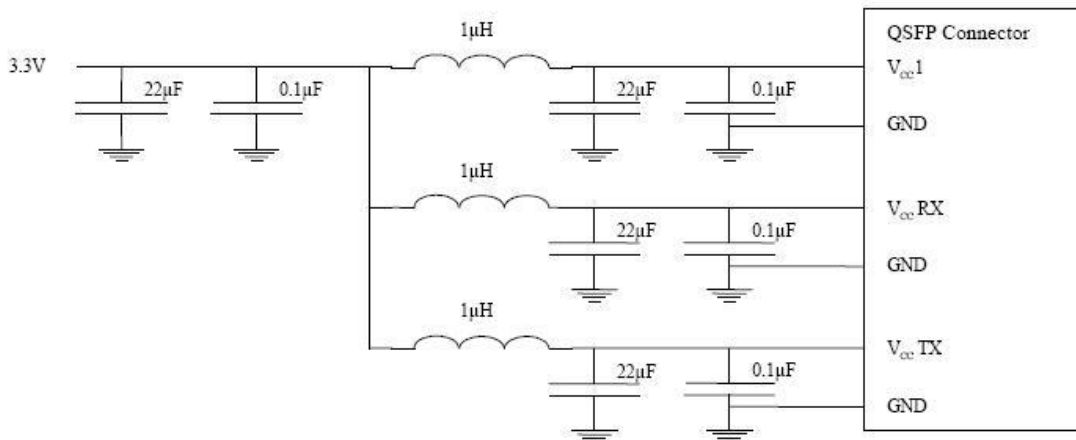

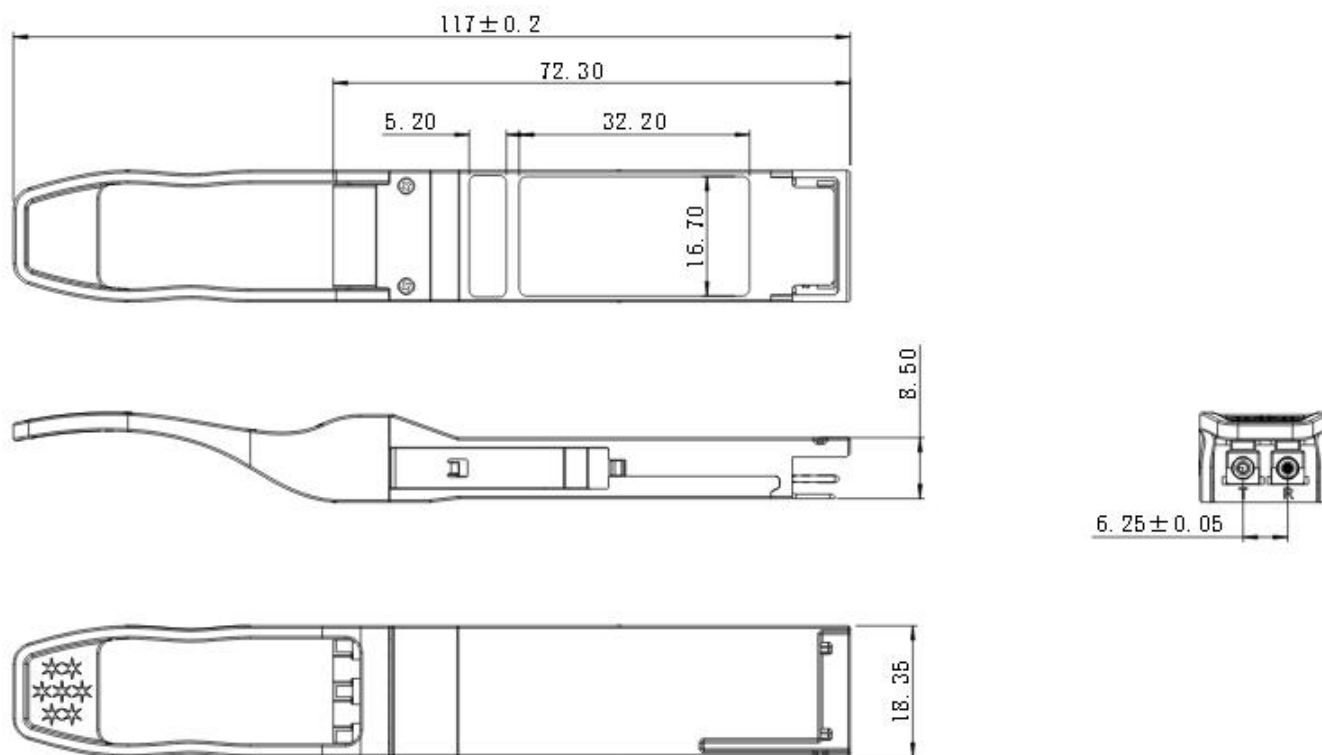Figure 7. Host Board Power Supply Filtering

Mechanical Dimensions

Figure 8. Mechanical Specifications

Regulatory Compliance

Gigalight GQS-MPO101-SR1 transceivers are Class 1 Laser Products. They meet the requirements of the following standards：

Feature	Standard
Laser Safety	IEC 60825-1:2014 (3rd Edition) IEC 60825-2:2004/AMD2:2010 EN 60825-1-2014 EN 60825-2:2004+A1+A2
Electrical Safety	EN 62368-1: 2014 IEC 62368-1:2014 UL 62368-1:2014
Environmental protection	Directive 2011/65/EU with amendment(EU)2015/863
CE EMC	EN55032：2015 EN55035：2017 EN61000-3-2:2014 EN61000-3-3:2013
FCC	FCC Part 15, Subpart B ANSI C63.4-2014

深圳市易飞扬通信技术有限公司
Shenzhen Gigalight Technology Co., Ltd.

www.gigalight.com · Optical Interconnection Design Innovator

References

1. QSFP28 MSA

2. SFF-8436 QSFP+

3. IEEE802.3db 100GBASE-SR1

⚠️**CAUTION:**

Use of controls or adjustment or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Ordering information

Part Number	Product Description
GQS-MPO101-SR1	QSFP28 SR1 106.25Gb/s, 850nm, OM4, MMF 100m, DDM, 0ºC ~ +70ºC

Important Notice

Performance figures,data and any illustrative material provided in this data sheet are typical and must be specifically confirmed in writing by Gigalight before they become applicable to any particular order or contract. In accordance with the Gigalight policy of continuous improvement specifications may change without notice.

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E-mail: sales@gigalight.com
Official Site: www.gigalight.com

Revision History

Revision	Date	Description
V0	Jun-06-2025	Advance Release.