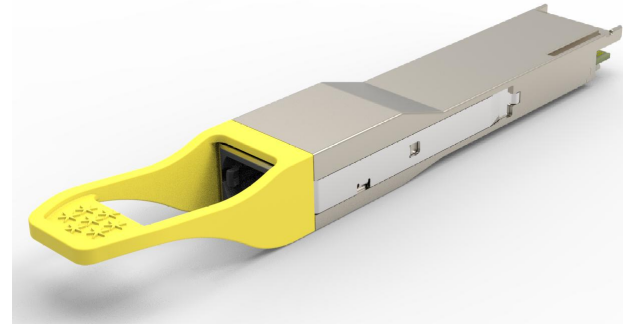


GIGALIGHT 400G QSFP112 DR4+ 2km Silicon Photonics Transceiver Module

P/N: GQS-SI401IR4C

Features

- ✓ QSFP112 MSA and CMIS compliant
- ✓ 4x106.25Gbps(53.125GBd PAM4)electrical interface
- ✓ 4x106.25Gbps(53.125GBd PAM4)optics architecture
- ✓ Power consumption <10W
- ✓ Maximum link length of 2km G.652 SMF with KP-FEC
- ✓ MPO-12 receptacles
- ✓ Built-in digital diagnostic functions
- ✓ Operating case temperature 0°C to +70°C
- ✓ 3.3V power supply voltage
- ✓ RoHS compliant(lead free)



Applications

- ✓ 400GBASE-DR4+
- ✓ InfiniBand NDR
- ✓ Data center network

Description

The Gigalight GQS-SI401IR4C is a transceiver module designed for 2km optical communication applications, and it is compliant to QSFP112 MSA, IEEE 802.3cu protocol. The silicon photonics transceiver is based on a new state-of-the-art silicon photonics (SiPh) platform. It uses SiPh chips that integrate a number of active and passive optoelectronic components, 3D packaging technology and industry-leading 7nm DSP chips. It is a cost-effective and lower power consumption solution for 400GBASE data center. It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference. The module offers very high functionality and feature integration, accessible via a two-wire serial interface.

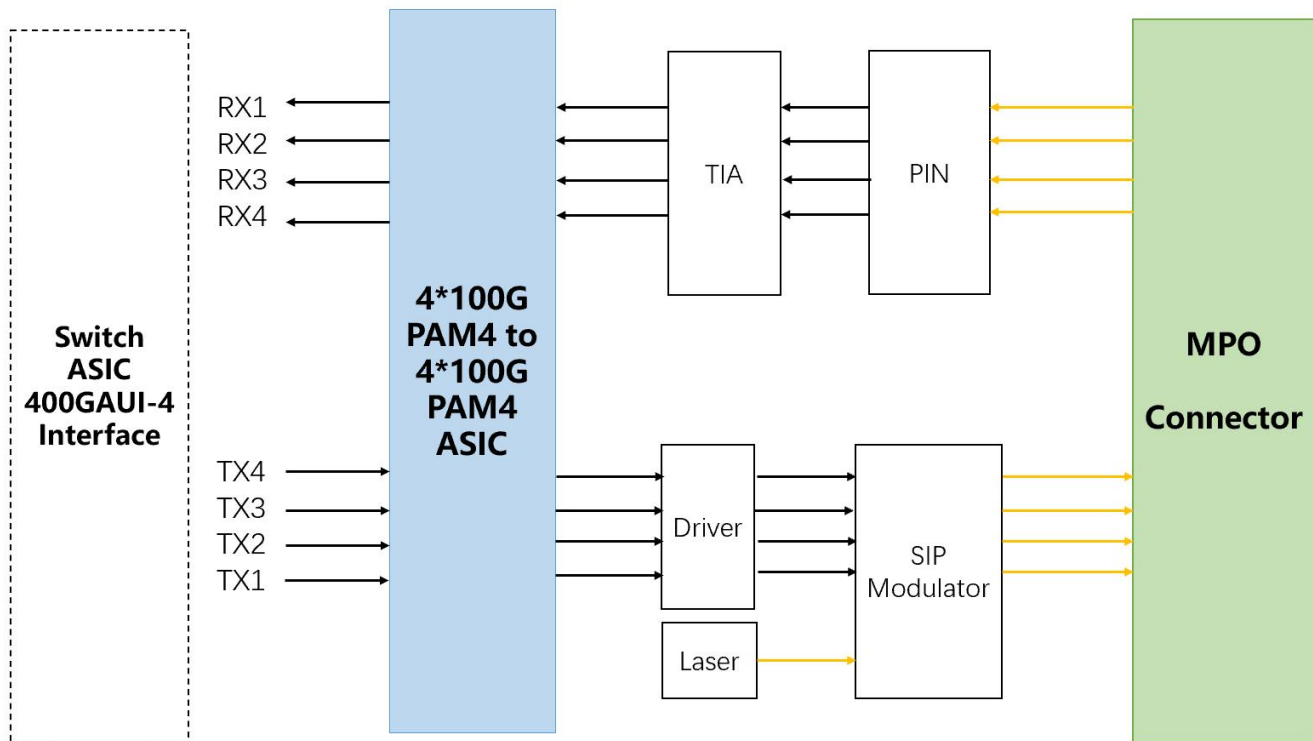


Figure1. Module Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	Vcc	-0.3	3.6	V
Input Voltage	Vin	-0.3	Vcc+0.3	V
Storage Temperature	Tst	-40	85	°C
Case Operating Temperature	Top	0	70	°C
Humidity(non-condensing)	Rh	5	95	%

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	Vcc	3.13	3.3	3.47	V
Operating Case temperature	Tca	0		70	°C
Data Rate Per Lane	fd		106.25		Gbit/s
Humidity	Rh	5		85	%
Power Dissipation	Pm			10	W

Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Differential input impedance	Zin	90	100	110	ohm
Differential Output impedance	Zout	90	100	110	ohm
Differential input voltage amplitude	ΔV_{in}	900			mVp-p
Differential output voltage amplitude	ΔV_{out}			900	mVp-p
Bit Error Rate	BER			2.4E-4	-
Transition Time		8			ps
Near-end Vertical Eye Closure over +/- 50 mUI (VEC)		12			UI
Near-end Vertical Eye Opening over +/- 50 mUI (VEO)		20			mV
Far-end Vertical Eye Closure over +/- 50 mUI (VEC)		12			UI
Far-end Vertical Eye Opening over +/- 50 mUI (VEO)		15			mV

Note:

- 1) BER=2.4E-4; PRBS31Q@53.125GBd. Pre-FEC
- 2) Differential input voltage amplitude is measured between TxnP and TxnN.
- 3) Differential output voltage amplitude is measured between RxnP and RxnN.

Optical Characteristics

Table 3 - Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Transmitter						
Centre Wavelength	λ_c	1304.5		1317.5	nm	-
Side-mode suppression ratio	SMSR	30	-	--	dB	-
Average launch power, each lane	Pout	-2.4	-	4.0	dBm	-
Optical Modulation Amplitude(OMA outer), each lane	OMA	-0.2	-	4.2	dBm	-

Transmitter and dispersion eye closure for PAM4 (TDECQ), each lane	TDECQ			3.4	dB	
Extinction Ratio	ER	3.5	-	-	dB	-
Average launch power of OFF transmitter, each lane				-15	dB	-
Receiver						
Centre Wavelength	λ_c	1304.5		1317.5	nm	-
Receiver Sensitivity in OMA outer	RXsen			-4.6	dBm	1
Average power at receiver, each lane input, each lane	Pin	-6.4		4.5	dBm	-
Receiver Reflectance				-26	dB	-
LOS Assert		-12			dBm	-
LOS De-Assert				-10	dBm	-
LOS Hysteresis		0.5			dB	-

Note:

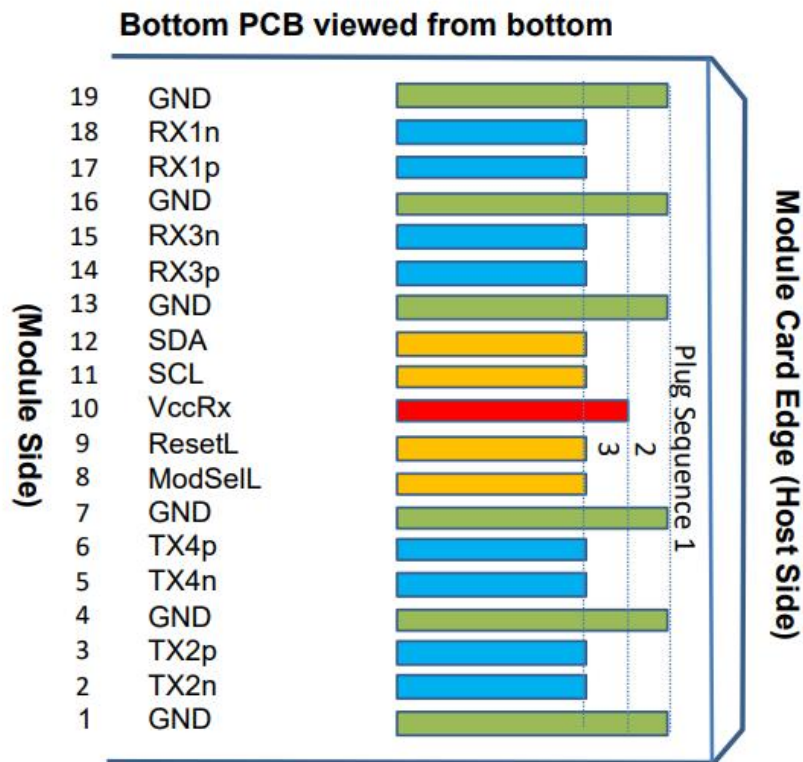
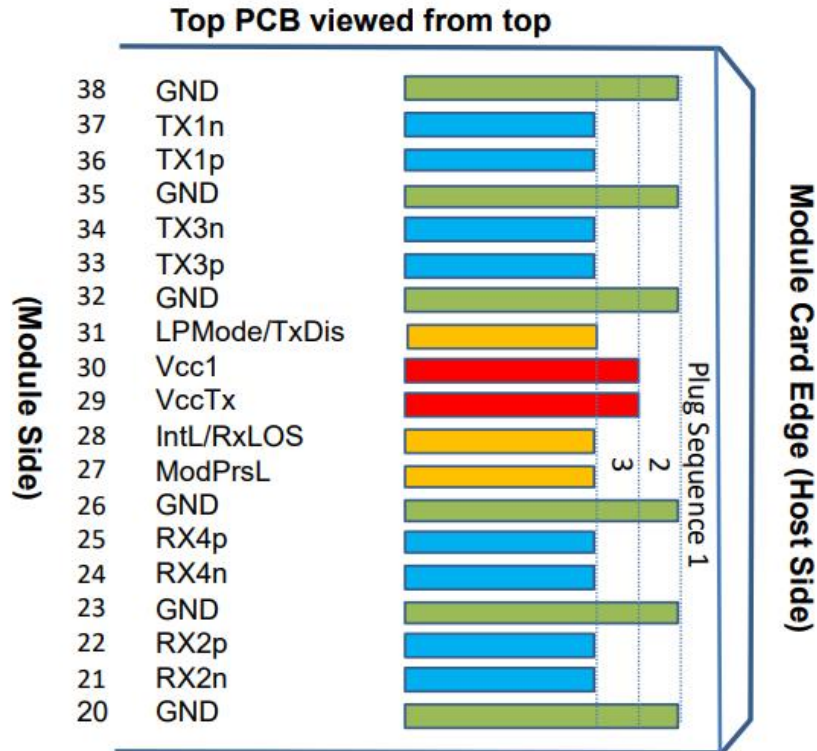
- 1) Measured with conformance test signal at TP3 for BER = 2.4E-4 Pre-FEC

Pin Description

Pad	Logic	Symbol	Description	Plug Sequence ⁴	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		VccRx	+3.3V Power Supply Receiver	2	2
11	LVC MOS-I/O	SCL	TWI serial interface clock	3	
12	LVC MOS-I/O	SDA	TWI serial interface data	3	
13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL/ RxLOS	Interrupt/optional RxLOS	3	
29		VccTx	+3.3V Power supply transmitter	2	2
30		Vcc1	+3.3V Power supply	2	2
31	LVTTL-I	LPMODE/ TxDis	Low Power mode/optional TX Disable	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1

Note 1: QSFP112 uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane. Each connector Gnd contact is rated for a maximum current of 500 mA. Note 2: VccRx, Vcc1, and VccTx shall be applied concurrently. Supply requirements defined for the host side of the Host Card Edge Connector are listed in Table 13. For power classes 4 and above the module differential loading of input voltage pads must not result in exceeding contact current limits. Each connector Vcc contact is rated for a maximum current of 1500 mA.

Note 4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1, 2, and 3 see Figure 14 for pad locations.



Classic
QSFP+/QSFP28/QSFP112 Pads

Figure2. Electrical Pin-out Details

ModSelL Pin

The ModSelL is an input signal that shall be pulled to Vcc in the QSFP112 modules. When held low by the host, the module responds to TWI serial communication commands. The ModSelL allows the use of multiple QSFP112 modules on a single TWI interface bus. When ModSelL is “High”, the module shall not respond to or acknowledge any TWI interface communication from the host.

In order to avoid conflicts, the host system shall not attempt TWI interface communications within the ModSelL de-assert time after any QSFP112 modules are deselected. Similarly, the host must wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de asserting periods of different modules may overlap as long as the above timing requirements are met.

ResetL Pin

The ResetL signal shall be pulled to Vcc in the module. A low level on the ResetL signal for longer than the minimum pulse length ($t_{\text{Reset_init}}$) initiates a complete module reset, returning all user module settings to their default state.

LPMODE/TxDis Pin

LPMODE/TxDis is a dual-mode input signal from the host operating with active high logic. It shall be pulled towards Vcc in the module. At power-up or after ResetL is deasserted LPMODE/TxDis behaves as LPMODE. If supported, LPMODE/TxDis can be configured as TxDis using the TWI interface except during the execution of a reset.

ModPrsL Pin

ModPrsL shall be pulled up to Vcc Host on the host board and pulled low in the module. The ModPrsL is asserted “Low” when the module is inserted. The ModPrsL is deasserted “High” when the module is physically absent from the host connector due to the pull-up resistor on the host board.

IntL/RxLOSL Pin

IntL/RxLOSL is a dual-mode active-low, open-collector output signal from the module. It shall be pulled up towards Vcc on the host board. At power-up or after ResetL is released to high, IntL/RxLOSL is configured as IntL. When the IntL signal is asserted Low it indicates a change in module state, a possible module operational fault or a status critical to the host system. The host identifies the source of

the interrupt using the TWI serial interface. The IntL signal is deasserted “High” after all set interrupt flags are read. If dual mode operation supported, IntL/RxLOSL can be optionally programmed as RxLOSL using the TWI interface except during the execution of a reset. If the module has no interrupt flags asserted (IntL/RxLOSL is high), there should be no change in IntL/RxLOSL states after the mode change.

Power Supply Filtering

The host board should use the power supply filtering shown in Figure3.

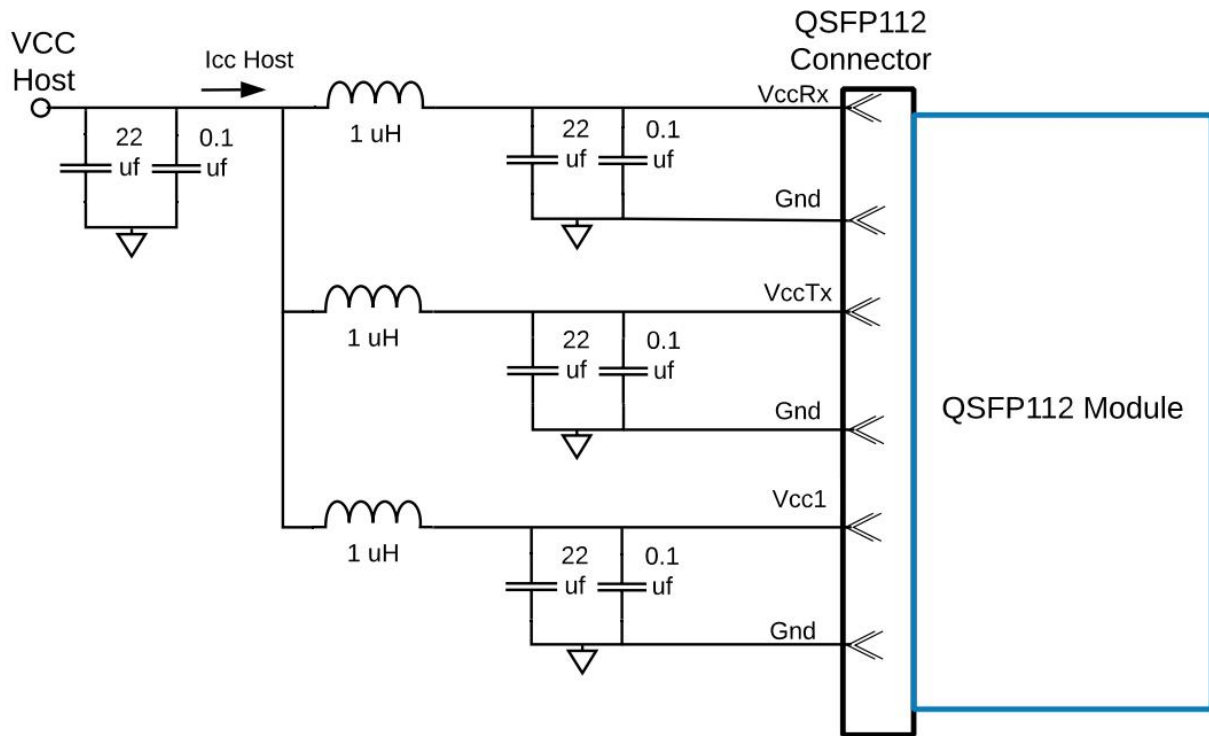


Figure3. Host Board Power Supply Filtering

DIAGNOSTIC MONITORING INTERFACE

Digital diagnostics monitoring function is available on all Gigalight QSFP112 products. A 2-wire serial interface provides user to contact with module.

Memory Structure and Mapping

This limits the management memory that can be directly accessed by the host to 256 bytes, which is divided in Lower Memory (addresses 00h through 7Fh) and Upper Memory (addresses 80h through FFh).

A larger addressable management memory is required for all but the most basic modules. This is supported by a structure of 128-byte pages, together with a mechanism for dynamically mapping any of the 128-byte pages from a larger internal management memory space into Upper Memory the host addressable space.

The addressing structure of the additional internal management memory is shown in Figure 4 The management memory inside the module is arranged as a unique and always host accessible address space of 128 bytes (Lower Memory) and as multiple upper address subspaces of 128 bytes each (Pages), only one of which is selected as host visible in Upper Memory. A second level of Page selection is possible for Pages for which several instances exist (e.g. where a bank of pages with the same Page number exists).

This structure supports a flat 256 byte memory for passive copper modules and permits timely access to addresses in the Lower Memory, e.g. Flags and Monitors. Less time critical entries, e.g. serial ID information and threshold settings, are available with the Page Select function in the Lower Page. For more complex modules which require a larger amount of management memory the host needs to use dynamic mapping of the various Pages into the host addressable Upper Memory address space, whenever needed.

Note: The management memory map has been designed largely after the QSFP memory map. This memory map has been changed in order to accommodate 4 electrical lanes and to limit the required memory space. The single address approach is used as found in QSFP. Paging is used in order to enable time critical interactions between host and module.

Supported Pages

A basic 256 byte subset of the Management Memory Map is mandatory for all CMIS compliant devices. Other parts are only available for paged memory modules, or when advertised by the module. See CMIS V4.0 for details regarding the advertisement of supported management memory spaces.

In particular, support of the Lower Memory and of Page 00h is required for all modules, including passive copper cables. These pages are therefore always implemented. Additional support for Pages 01h, 02h and bank 0 of Pages 10h and 11h is required for all paged memory modules.

Bank 0 of pages 10h-1Fh, provides lane-specific registers for the first 4 lanes, and each additional bank provides support for additional 4 lanes. Note, however, that the allocation of information over the banks may be page specific and may not to be related to grouping data for 4 lanes.

The structure allows address space expansion for certain types of modules by allocating additional Pages. Moreover, additional banks of pages.

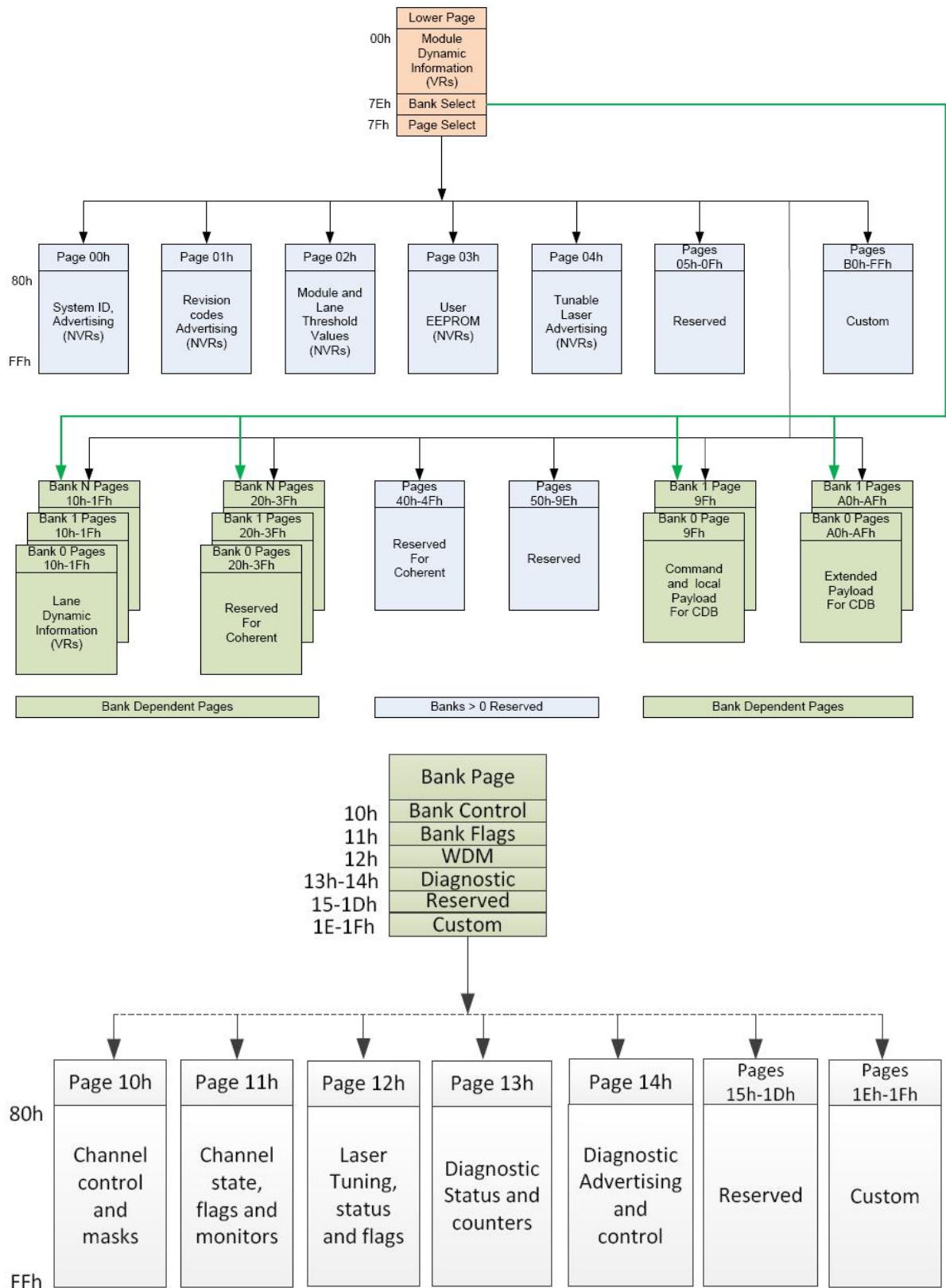


Figure4. QSFP12 Memory Map

Technical drawing of the MP012 module, showing three views: top, side, and bottom. The drawing includes dimensions and labels for components.

Top View Dimensions:

- Overall width: 18.35
- Overall length: 122.15
- Distance from left edge to first vertical divider: 87.14
- Distance from first vertical divider to second vertical divider: 2.4
- Distance from second vertical divider to third vertical divider: 16.7
- Distance from third vertical divider to right edge: 4.2
- Distance from left edge to first horizontal divider: 17
- Distance from first horizontal divider to second horizontal divider: 5.2
- Distance from second horizontal divider to right edge: 32.2
- Distance from right edge to bottom edge: 16.15

Side View Dimensions:

- Overall height: 13.1
- Distance from top edge to bottom edge of the main body: 3.2
- Distance from bottom edge of the main body to the bottom edge of the connector: 1.4
- Distance from bottom edge of the main body to the bottom edge of the connector: 0.6 ± 0.05
- Distance from bottom edge of the main body to the bottom edge of the connector: 2.25
- Distance from bottom edge of the main body to the bottom edge of the connector: 8.5
- Distance from bottom edge of the main body to the bottom edge of the connector: 1

Bottom View Dimensions and Labels:

- Overall width: 18.35
- Overall length: 122.15
- Distance from left edge to first vertical divider: 87.14
- Distance from first vertical divider to second vertical divider: 2.4
- Distance from second vertical divider to third vertical divider: 16.7
- Distance from third vertical divider to right edge: 4.2
- Distance from left edge to first horizontal divider: 17
- Distance from first horizontal divider to second horizontal divider: 5.2
- Distance from second horizontal divider to right edge: 32.2
- Distance from right edge to bottom edge: 16.15
- Labels: TX 1-4, RX 1-4, Key, MP012

FCC

FCC Part 15, Subpart B
ANSI C63.4-2014

References

1. QSFP112 MSA
2. CMIS
3. IEEE802.3cu
4. OIF CEI-112G-VSR

CAUTION:

Use of controls or adjustment or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Ordering information

Part Number	Product Description
GQS-SI401IR4C	QSFP112, 400GBASE-DR4+, 2km on Single mode Fiber (SMF), with DSP Power consumption <10W, MPO-12 connector.

Important Notice

Performance figures, data and any illustrative material provided in this data sheet are typical and must be specifically confirmed in writing by GIGALIGHT before they become applicable to any particular order or contract. In accordance with the GIGALIGHT policy of continuous improvement specifications may change without notice.

The publication of information in this data sheet does not imply freedom from patent or other protective rights of GIGALIGHT or others. Further details are available from any GIGALIGHT sales representative.

E-mail: sales@gigalight.com

Official Site: www.gigalight.com

Revision History

Revision	Date	Description
V0	Jul-29-2025	Advance Release.