

28G SFP28 Active Optical Cables

P/N: GSS-MDO280-xxxC (xxx: 001 to 100)

Features

- Transmission data rate up to 28.05Gbps
- 850nm VCSEL laser
- PIN photo-detector
- Internal CDR on both transmitter and receiver channels
- Low power consumption < 1W
- Hot-pluggable SFP28 form factor
- Up to 70m on OM3 MMF and 100m on OM4 MMF
- Digital diagnostics functions are available (optional)
- Operating case temperature range 0°C to +70°C
- 3.3V power supply voltage
- RoHS-6 compliant



Applications

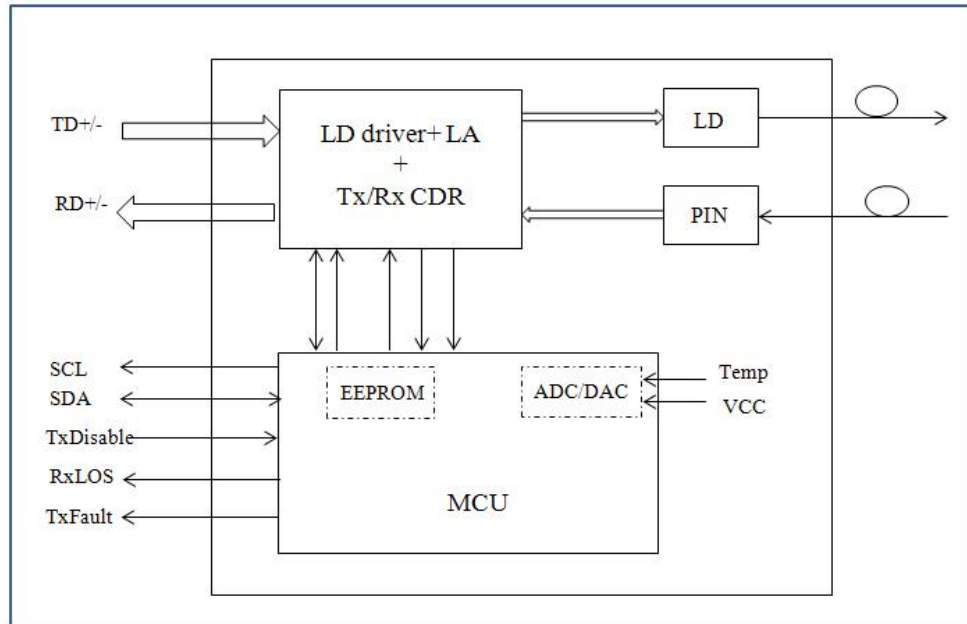
- Tri-rate 8G/16G/32G Fibre Channel

Description

The Gigalight 28G SFP28 Active Optical Cables (AOCs) are direct-attach fiber assemblies with SFP28 connectors, compliant with 8G/16G/32G Fibre Channel standards. They are suitable for short distances and offer a cost-effective solution to connect within racks and across adjacent racks. The length is up to 70 meters using OM3 MMF and 100 meters using OM4 MMF.

The 28G SFP28 AOC is designed to operate over multimode fiber systems using a nominal wavelength of 850nm. The electrical interface uses a 20-contact edge type connector.

Block Diagram



Absolute Maximum Ratings

Table 1 - Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	Vcc	0	3.6	V
Storage Temperature	Ts	-40	+85	°C
Operating Humidity	RH	5	85	%

Recommended Operating Conditions

Table 2 - Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Operating Case Temperature	Tc	0		+70	°C
Power Supply Voltage	Vcc	3.13	3.3	3.47	V
Power Supply Current	Icc			300	mA
Fiber Length on 50/125µm high-bandwidth (OM3) MMF				70	m
Fiber Length on 50/125µm high-bandwidth (OM4) MMF				100	m

Optical and Electrical Characteristics

Table 3 - Optical and Electrical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Transmitter						
Data rate	BR			28.05	Gbps	
Centre Wavelength	λ_c	840	850	860	nm	
Spectral Width (-20dB)	σ			0.6	nm	
Average Output Power	P _{avg}	-8.4		2.4	dBm	
Optical Power OMA	P _{OMA}	-6.4		3	dBm	
Extinction Ratio	ER	2			dB	
Differential data input swing	V _{IN,PP}	40		1000	mV	
Input Differential Impedance	Z _{IN}	90	100	110	Ω	
TX Disable	Disable		2.0	V _{cc}	V	
	Enable		0	0.8	V	
TX Fault	Fault		2.0	V _{cc}	V	
	Normal		0	0.8	V	
Receiver						
Data rate	BR			28.05	Gbps	
Centre Wavelength	λ_c	840	850	860	nm	
Unstressed Receiver Sensitivity (OMA) 8.5Gb/s 14.025Gb/s 28.05Gb/s	P _{sens}	-	-	-11.2 -10.5 -10.2	dBm	
Receiver Power (OMA)				3	dBm	
LOS De-Assert	LOS _D			-13	dBm	
LOS Assert	LOS _A	-30			dBm	
LOS Hysteresis		0.5			dB	
Differential data output swing	V _{out,PP}	300		850	mV	
LOS	High	2.0		V _{cc}	V	
	Low			0.8	V	

Notes:

1.For 32GFC with TEC, receive sensitivity is defined at 10⁻⁶ BER level.

Timing and Electrical

Table 4 - Timing and Electrical

<i>Parameter</i>	<i>Symbol</i>	<i>Min.</i>	<i>Max.</i>	<i>Unit</i>	<i>Conditions</i>
Tx_Disable assert time	t_off		100	μs	Rising edge of Tx_Disable to fall of output signal below 10% of nominal
Tx_Disable negate time	t_on		2	ms	Falling edge of Tx_Disable to rise of output signal above 90% of nominal. This only applies in normal operation, not during start up or fault recovery.
Time to initialize 2-wire interface	t_2w_start_up		300	ms	From power on or hot plug after the supply meeting Table 8.
Time to initialize	t_start_up		300	ms	From power supplies meeting Table 8 or hot plug or Tx disable negated during power up, or Tx_Fault recovery, until non-cooled power level I part (or non-cooled power level II part already enabled at power level II for Tx_Fault recovery) is fully operational.
Time to initialize cooled module and time to power up a cooled module to Power Level II	t_start_up_cooled		90	s	From power supplies meeting Table 8 or hot plug, or Tx disable negated during power up or Tx_Fault recovery, until cooled power level I part (or cooled power level II part during fault recovery) is fully operational. Also, from stop bit low-to-high SDA transition enabling Power Level II until cooled module is fully operational
Time to Power Up to Level II	t_power_level2		300	ms	From stop bit low-to-high SDA transition enabling power level II until non-cooled module is fully operational
Time to Power Down from Level II	t_power_down		300	ms	From stop bit low-to-high SDA transition disabling power level II until module is within power level I requirements
Tx_Fault assert	Tx_Fault_on		1	ms	From occurrence of fault to assertion of Tx_Fault
Tx_Fault assert for cooled module	Tx_Fault_on_cooled		50	ms	From occurrence of fault to assertion of Tx_Fault
Tx_Fault Reset	t_reset	10		μs	Time Tx_Disable must be held high to reset Tx_Fault
RS0, RS1 rate select timing for FC	t_RS0_FC, t_RS1_FC		500	μs	From assertion till stable output
RS0, RS1 rate select timing non FC	t_RS0, t_RS1		24	ms	From assertion till stable output
Rx_LOS assert delay	t_los_on		100	μs	From occurrence of loss of signal to assertion of Rx_LOS
Rx_LOS negate delay	t_los_off		100	μs	From occurrence of presence of signal to negation of Rx_LOS

Diagnostics

Table 5 – Diagnostics Specification

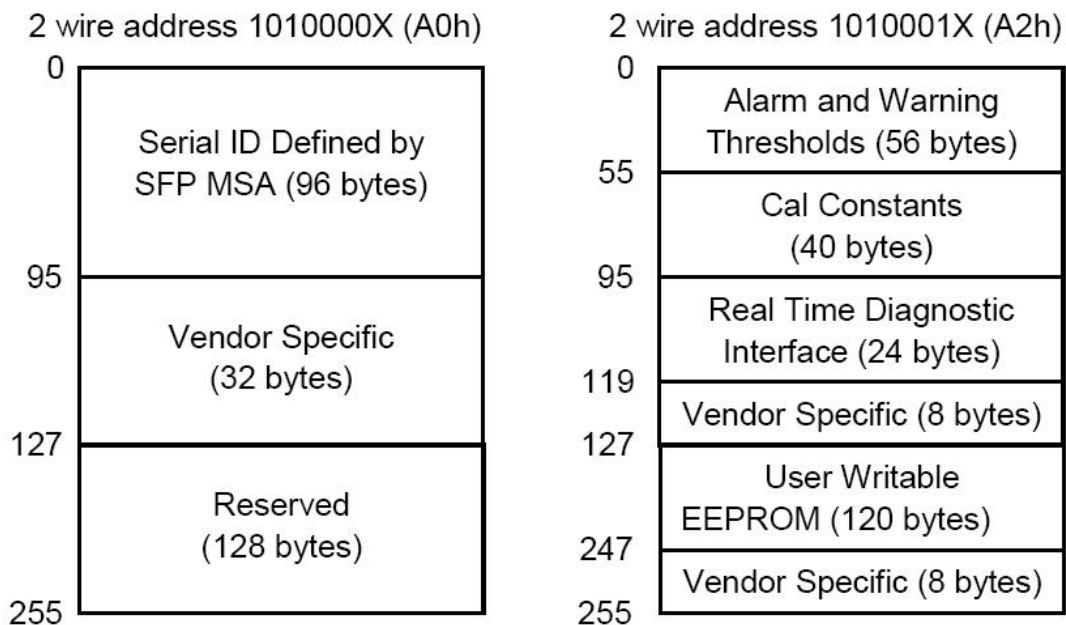
Parameter	Range	Unit	Accuracy	Calibration
Temperature	0 to +70	°C	±5°C	Internal / External
Voltage	3.0 to 3.6	V	±3%	Internal / External
Bias Current	0 to 20	mA	±10%	Internal / External
TX Power	-8 to 3	dBm	±3dB	Internal / External
RX Power	-14 to 0	dBm	±3dB	Internal / External

Digital Diagnostic Memory Map

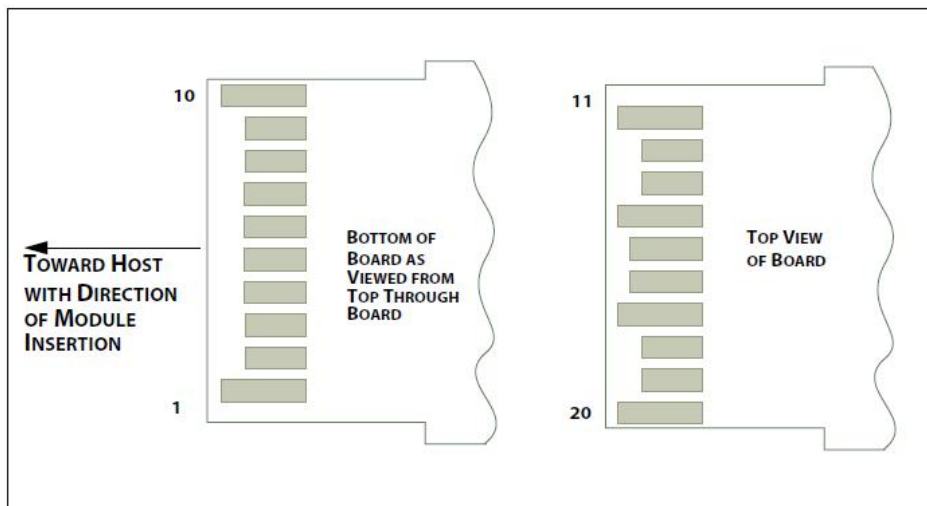
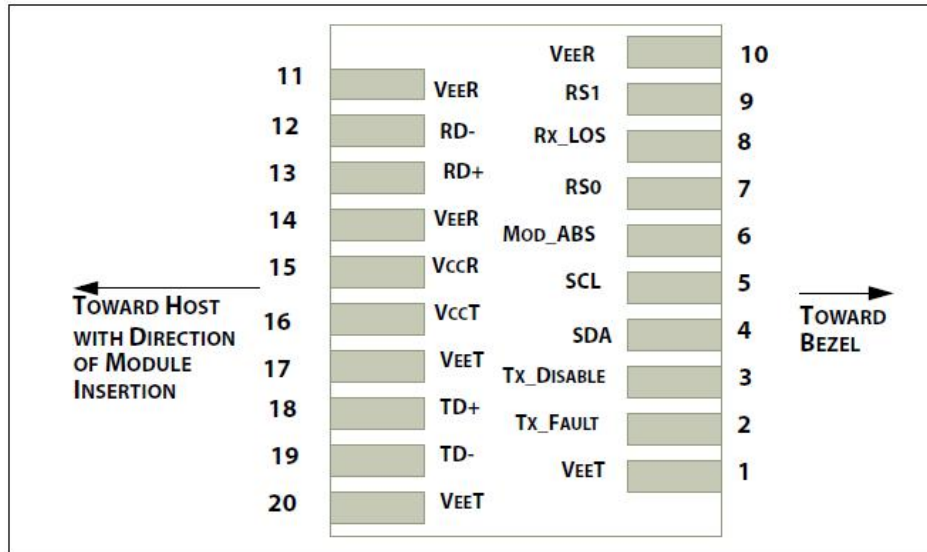
The transceivers provide serial ID memory contents and diagnostic information about the present operating conditions by the 2-wire serial interface (SCL, SDA).

The diagnostic information with internal calibration or external calibration all are implemented, including received power monitoring, transmitted power monitoring, bias current monitoring, supply voltage monitoring and temperature monitoring.

The digital diagnostic memory map specific data field defines as following.



Pin Definitions



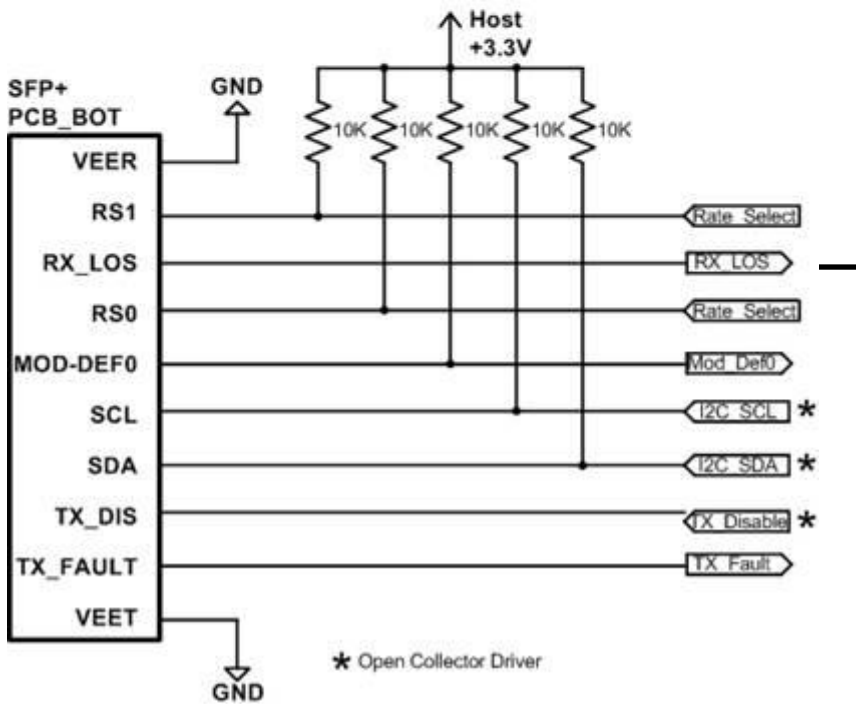
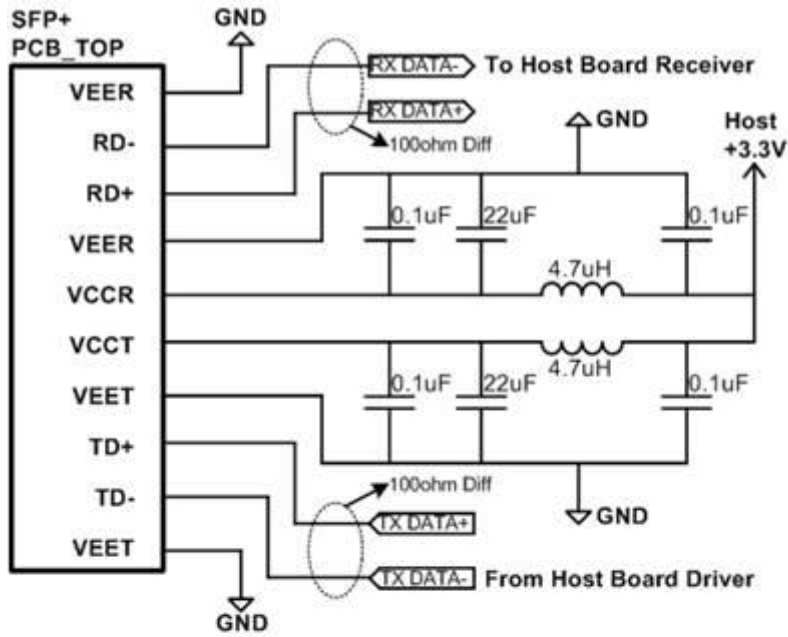
Pin Descriptions

PIN	Logic	Symbol	Name / Description	Note
1		VeeT	Module Transmitter Ground	1
2	LVTTL-O	TX_Fault	Module Transmitter Fault	2
3	LVTTL-I	TX_Dis	Transmitter Disable; Turns off transmitter laser output	
4	LVTTL-I/O	SDA	2-Wire Serial Interface Data Line	2
5	LVTTL-I	SCL	2-Wire Serial Interface Clock	2
6		MOD_ABS	Module Definition, Grounded in the module	
7	LVTTL-I	RS0	Receiver Rate Select	
8	LVTTL-O	RX_LOS	Receiver Loss of Signal Indication Active LOW	
9	LVTTL-I	RS1	Transmitter Rate Select (not used)	
10		VeeR	Module Receiver Ground	1
11		VeeR	Module Receiver Ground	1
12	CML-O	RD-	Receiver Inverted Data Output	
13	CML-O	RD+	Receiver Data Output	
14		VeeR	Module Receiver Ground	1
15		VccR	Module Receiver 3.3 V Supply	
16		VccT	Module Receiver 3.3 V Supply	
17		VeeT	Module Transmitter Ground	1
18	CML-I	TD+	Transmitter Non-Inverted Data Input	
19	CML-I	TD-	Transmitter Inverted Data Input	
20		VeeT	Module Transmitter Ground	1

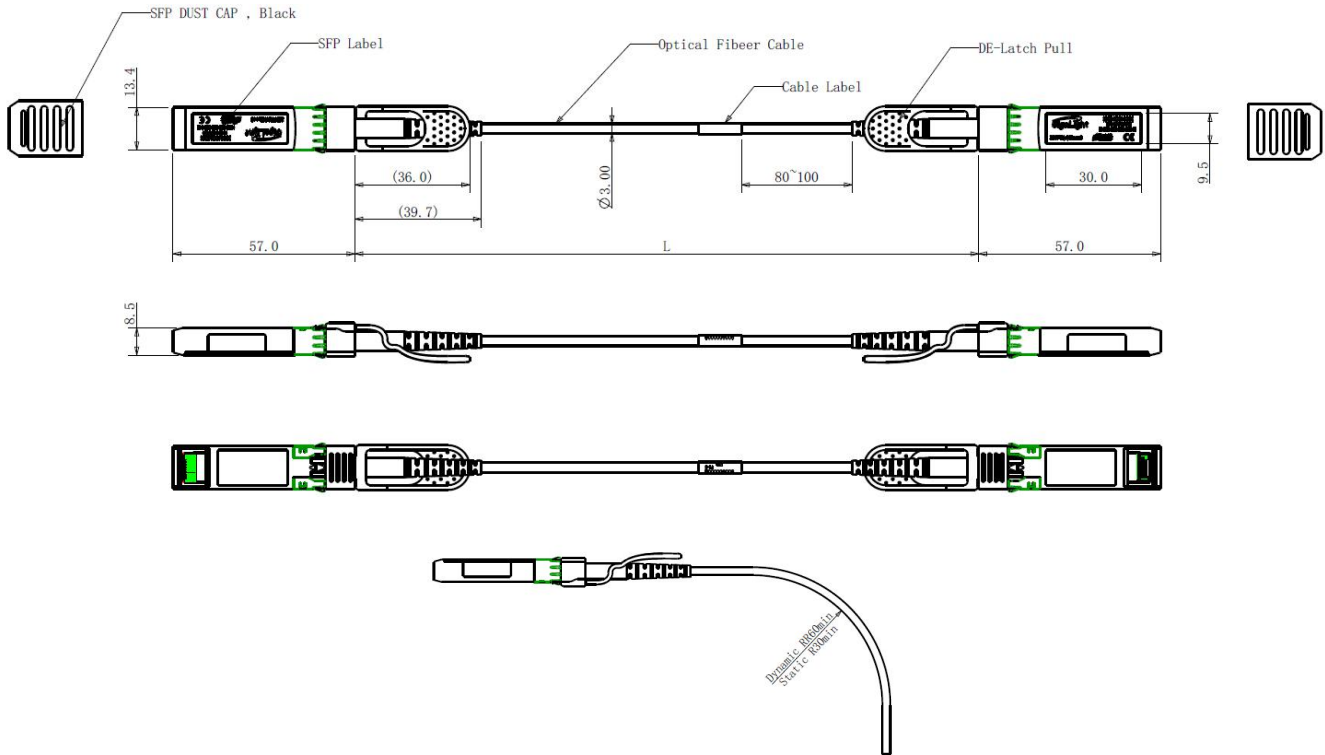
Notes:

1. Module ground pins GND are isolated from the module case.
2. Shall be pulled up with 4.7K-10Kohms to a voltage between 3.15V and 3.45V on the host board.

Recommended Interface Circuit



Mechanical Dimensions



Ordering information

Part Number	Product Description
GSS-MDO280-xxxC	28G SFP28 Active Optical Cables, 28Gb/s, 0°C to +70°C
xxx: 001 to 070, 1 to 70 length in meters on OM3 MMF	
xxx: 001 to 100, 1 to 100 length in meters on OM4 MMF	
Further details are available from any Gigalight sales representative.	

E-mail: sales@gigalight.com

Web : <https://www.gigalight.com/>