100G CFP-DCO Digital Coherent Optical Transceiver

Features

- Operating optical data rate up to 128Gbps
- Transmission distance up to 1200km
- CD tolerance 40000ps/nm
- DGD tolerance 50ps
- Low latency HFEC/SDFEC
- CFP MSA compliant
- IEEE 802.3ba MAC compliant
- OTU4 and 100GE compatible
- OTL4.10 and CAUI compatible
- Full C-Band 50GHz ITU-T transmitter
- Built in Client and line OTN Processing
- Hot-pluggable electrical interface
- Typical power dissipation 23/28W
- Duplex LC receptacles
- Operating case temperature range 0°C to +70°C
- 3.3V power supply voltage
- RoHS-6 compliant (lead free)
- PRBS generation and detection for line and host interfaces
- ZR/MR/LH options
- Single ITLA

Applications

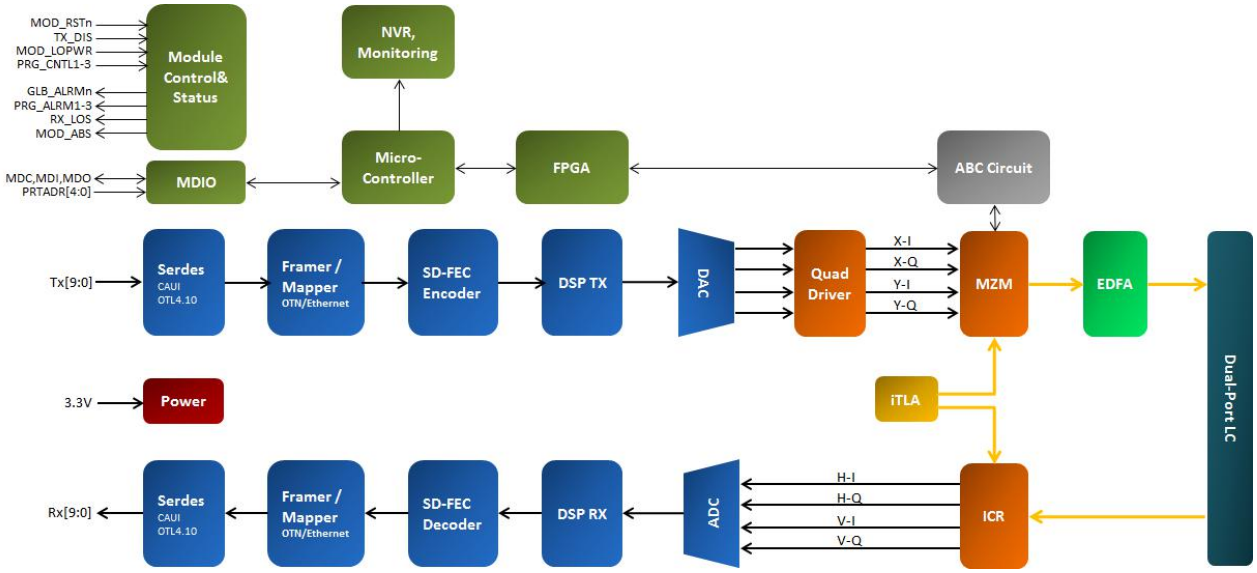
- 100GbE IEEE 802.3bj
- ITU-T G.709/Y.1331 for OTN
- Switch to switch interface or switch to router interface
- Access/Metro/Long-haul Ethernet DWDM networks

Description

The Gigalight 100G CFP-DCO digital coherent optical transceiver is a hot-pluggable CFP form-factor optical module designed for high-speed optical networking applications including 100-Gigabit Ethernet and OTU4.

The CAUI and OTL4.10 electrical interface and MDIO management interface are built in the module. The module converts 10-lane 10Gb/s electrical data streams to 128G DP-QPSK optical output signal in Egress, and also converts DP-QPSK optical input signals to 10-lane 10Gb/s electrical data streams in ingress. This 10-lane 10Gb/s electrical signal is fully compliant with 802.3ba CAUI specification and OIF-CEI-03.1 specification, and allows FR4 host PCB trace up to 25cm.

The block diagram is shown below. One chip called DSP is used for electric data signals Mux/ Demux. Driver is used for up to 28G electric signal amplify. ITLA is a full C_Band wavelength tunable assemble used for optical signal carrier in egress and for coherent receive in ingress. MZM is used for E-O convert in egress and ICR is used for O-E convert in ingress. The optical signals format is DP-QPSK. EDFA is used for optical signal amplify to get suitable output optical power.



Module Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	Unit	Min	Max
Storage Temperature Range	T_s	℃	-40	+85
Relative Humidity	RH	%	5	85
Power Supply Voltage	V_{cc}	V	-0.5	+ 3.6
Operating Case Temperature Range	T_c	℃	-5	75
Receiver Optical Power	P_{dag}	dBm		+3

Recommended Operating Conditions

Parameter	Symbol	Unit	Min	Typ	Max
Operating Case Temperature Range	T_c	℃	0		70
Power Supply Voltage	V_{cc}	V	3.2	3.3	3.4
Data rate		Gb/s		103.125	112

Products Characteristics

(Tested under recommended operating conditions)

Parameter	Symbol	Unit	Min	Typ	Max	Notes
Voltage Supply Electrical Characteristics						
Supply Current		A	-	-	10	
Power Supply Noise	V_{rip}				2%	DC-1MHz
					3%	1-10MHz
Dissipation Class3/4	P_w	W		28	30	LH
				22	24	MR
				21	23	ZR
Low Power Dissipation	P_{low}	W			2	
Inrush Current $_{n\,2}$	I-inrush mA/usec				100	
Turn-off Current ^{Class2}	I-turnoff mA/usec		-100			

Different Signal Electrical Characteristics						
Single Ended Data Input Swing		mV	55 -		525	
Single Ended Data Output Swing		mV	180 -		385	
Differential Signal Resistance	Output	Ω	80		120	
Differential Signal Resistance	Input	Ω	80		120	
3.3V LVCMOS Electrical Characteristics						
Input High Voltage	$3.3V_{IH}$	V	2.0		V_{cc}+0.3	
Input Low Voltage	$3.3V_{IL}$	V	-0.3 -		0.8	
Input Leakage Current	$3.3I_{IN}$	uA	-10		+ 10	
Output HighVoltage(I_{OH}=100uA)	$3.3V_{OH}$	V	V_{cc}-0.2 -		-	
Output Low Voltage (I_{OI} = 100uA)	$3.3V_{OL}$	V			0.2	
Minimum Pulse Width of Control Pin Signal	T_CNTL	us	100			
1.2V LVCMOS Electrical Characteristics						
Input High Voltage	$1.2V_{IH}$	V	0.84		1.5	
Input Low Voltage	$1.2V_{IL}$	V	-0.3		0.36	
Input Leakage Current	$1.2I_{IN}$	uA	-100		+ 100	
Output HiqhVoltaqe	$1.2V_{OH}$	V	1.0		1.5	
Output Low Voltaqe	$1.2V_{OL}$	V	-0.3		0.2	
Output Hiqh Current	$1.2I_{OH}$	mA			-4	
Output Low Current	$1.2I_{OL}$	mA	+4			
Input Capacitance	C_i	pF			10	
Optical Transmitter Characteristics						
Signaling Rate for Each Lane (100GbE)		Gbps	-	25.78125+/-100ppm		
Signaling Rate for Each Lane (OTU4)				27.95249+/-20ppm		
Wavelength Range	DWDM	nm	1527.60	-	1567.55	

Channel Spacing	$f_{SPACING}$	GHz	50			
Laser Tuning Range	f_{TUNE}		Full C-band			
Wavelength Accuracy	λ_{EOL}	GHz	-1.8	-	+1.8	
Output Power (adjustable)	P_{OUT}	dBm	-15	-	+1	With VOA
Output Power Accuracy		dB	-1		1	BOL
Output Power Stability	Short time	dB	-0.3		0.3	
Shutdown Optical Power	P_{OFF}	dBm			-40	
Spectral Width @-20dB		GHz			40	
Transmitter Warm-Start Ready Time		ms		100		
Transmitter Cold-start Ready Time		s		120		
Transmitter OSNR		dB/0.1nm	35			
Transmitter Polarization Imbalance		dB			1	
Optical Receiver Characteristics						
Receive Rate for Each Lane(100GbE)		Gbps		25.78125+/-100ppm		
Receive Rate for EachLane(OTU4)				27.95249+/-20ppm		
Wavelength Range	DWDM	nm	1527.60	-	1567.55	
Receiver Operating Range	P_w	dBm	-18	-	0	
Receiver B2B Optical power Sensitivity	O_sense	dBm	-21			
ZR OSNR（@BER=4E-3）	$OSNR_{MIN}$	dB/0.1nm	17			HFEC

MR OSNR (@BER=4E-3)	$OSNR_{MIN}$	dB/0.1nm	15.5			HFEC
LH OSNR (@BER=2e-2)	$OSNR_{MIN}$	dB/0.1nm	13			SD-FEC
Chromatic Dispersion Compensation	CD	ps/nm			12000	ZR
		ps/nm			25000	MR
		ps/nm			40000	LH
Filter Tolerance	OTF	GHz	30	45		
Optical Input Transient tolerance		dB			3	
PMD Capability (DGD)	DGD	ps			50	
PDL Tolerance	PDL	dB			3	
Polarization SOP Tracking	SOP	kHz		20	20	
Receiver Warm-Start Turn-Up Time		s			30	
Receiver Cold-Start Turn-Up Time		s		60		
OSNR Sensitivity for Clock Recovery	dB/0.1nm	12			dB/0.1nm	

Note1. The supply current includes CFP module's supply current and test board working current.

Hardware Control Pins

The CFP Module support real-time control functions via hardware pins, listed in the following table: Hardware Control Pins

Pin#	Symbol	Description	I/O	Logic	H	L	Pull-up/down
30	PRG_CNTL1	Programmable Control 1 MSADefault: TRXIC_RST n , TX&RX ICs reset, “0〃:reset; “1”	I	3.3V LVCMOS	per CFP MSA Management Interface Specification		Pull-Up Note1
31	PRG_CNTL2	Programmable Control 2 MSADefault : Hardware Interlock LSB	I	3.3V LVCMOS			Pull-Up Note1
32	PRG_CNTL3	Programmable Control 3 MSA Default:Hardware Interlock MSB	I	3.3V LVCMOS			Pull-Up Note1
36	TX_DIS	Transmitter Disable	I	3.3V LVCMOS	Disable	Enable	Pull-Up Note1
37	MOD_LOPWR	Module Low Power Mode	I	3.3V LVCMOS	Low Power	Enable	Pull-Up Note1
39	MOD_RSTn	Module Reset(Invert)	I	3.3V LVCMOS	Enable	Reset	Pull-Down Note2

Hardware Alarm Pins

The CFP Module supports alarm hardware pins listed in the following table: Hardware Alarm Pins

Pin#	Symbol	Description	I/O	Logic	H	L	Pull-up/down
33	PRG ALRM 1	Programmable Alarm 1 MSADefault:HIPWR_ON	O	3.3V LVCMOS	Active High per MDIO document		
34	PRG ALRM 2	Programmable Alarm 2MSA default:MOD_READY , Ready State has been reached	O	3.3V LVCMOS			
35	PRG ALRM3	Programmable Alarm 3 MSA Default: MOD FAULT	O	3.3V LVCMOS			
38	MOD_ABS	Module Absent	O	3.3V LVCMOS	Absent	Present	Pull-Down Note1

40	RX_LOS	Receiver Loss of Signal	O	3.3V LVCMOS	Loss of Signal	OK	

Note1: Pull-Up resistor (4.7KOhm to 10 KOhm) is located within the CFP module Note2: Pull-Down resistor (4.7KOhm to 10 kOhm) is located within the CFP module

Management Interface Pins (MDIO)

The CFP Module supports alarm, control and monitor functions via an MDIO bus. The CFP MDIO pins are listed in the following table: Management Interface Pins

Pin#	Symbol	Description	I/O	Logic	H	L	Pull-up/down
41	GLB_ALRMn	Global Alarm	O	3.3V LVCMOS	Ok	Alarm	
47	MDIO	Management Data Input Output Bi-Directional Data	I/0	1.2V LVCMOS			
48	MDC	MDIO Clock	I	1.2V LVCMOS			
46	PRTADR0	MDIO Physical Port address bit0	I	1.2V LVCMOS	per MDIO document[5]		
45	PRTADR1	MDIO Physical Port address bit1	I	1.2V LVCMOS			
44	PRTADR2	MDIO Physical Port address bit2	I	1.2V LVCMOS			
43	PRTADR3	MDIO Physical Port address bit3	I	1.2V LVCMOS			
42	PRTADR4	MDIO Physical Port address bit4	I	1.2V LVCMOS			

Hardware Signaling Pin Timing Requirements

Timing Parameters for CFP hardware Signal Pins are listed in the following table.

Parameter	Symbol	Min	Max	Unit	Notes&Conditions
Hardware MOD_LOPWR assert	t_MOD_LOPWR_assert		10	ms	Application Specific May depend on current state Condition when signal is applied .See
TX Disable Assert Time	T_off		1	ms	

High Speed Electrical Characteristics

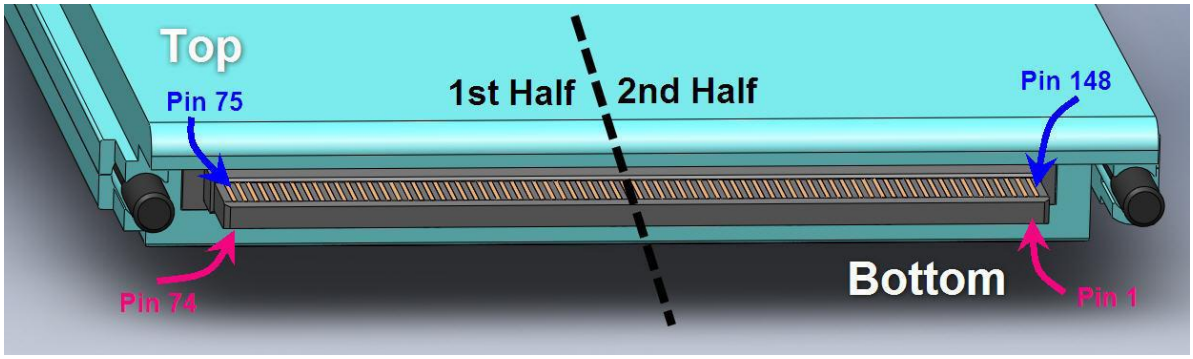
Reference Clock Characteristics

		Min	Typ	Max	Unit	Notes
Impedance	Z_d	80	100	120	Q	
Frequency			622.08		MHz	1/64 or 1/16 of electrical lane rate
Frequency Stability	△f	-100		100	ppm	For Ethernet applications
		-20		20		For Telecom applications
Output Differential Voltage	V_{DIFF}	400		1200	mV	Peak to Peak Differential
RMS jitter1-2	0			10	ps	Random Jitter Over frequency band of 10KHz<f<10MHz
Clock Duty Cycle		40		60	%	
Clock Rise/Fall Time 10%/90%	tr/f	200		1250	ps	1/64 of electrical lane rate
		50		315		1/16 of electrical lane rate

Note1: The

Optional Transmitter and Receiver Monitor Clock Characteristics

		Min	Typ	Max	Unit	Notes
Impedance	Z_d	80	100	120	Q	
Frequency					MHz	1/16 of Network lane rate
Output Differential Voltage	V_{DIFF}	400		1200	mV	Peak to Peak Differential
Clock Duty Cycle		40		60	%	

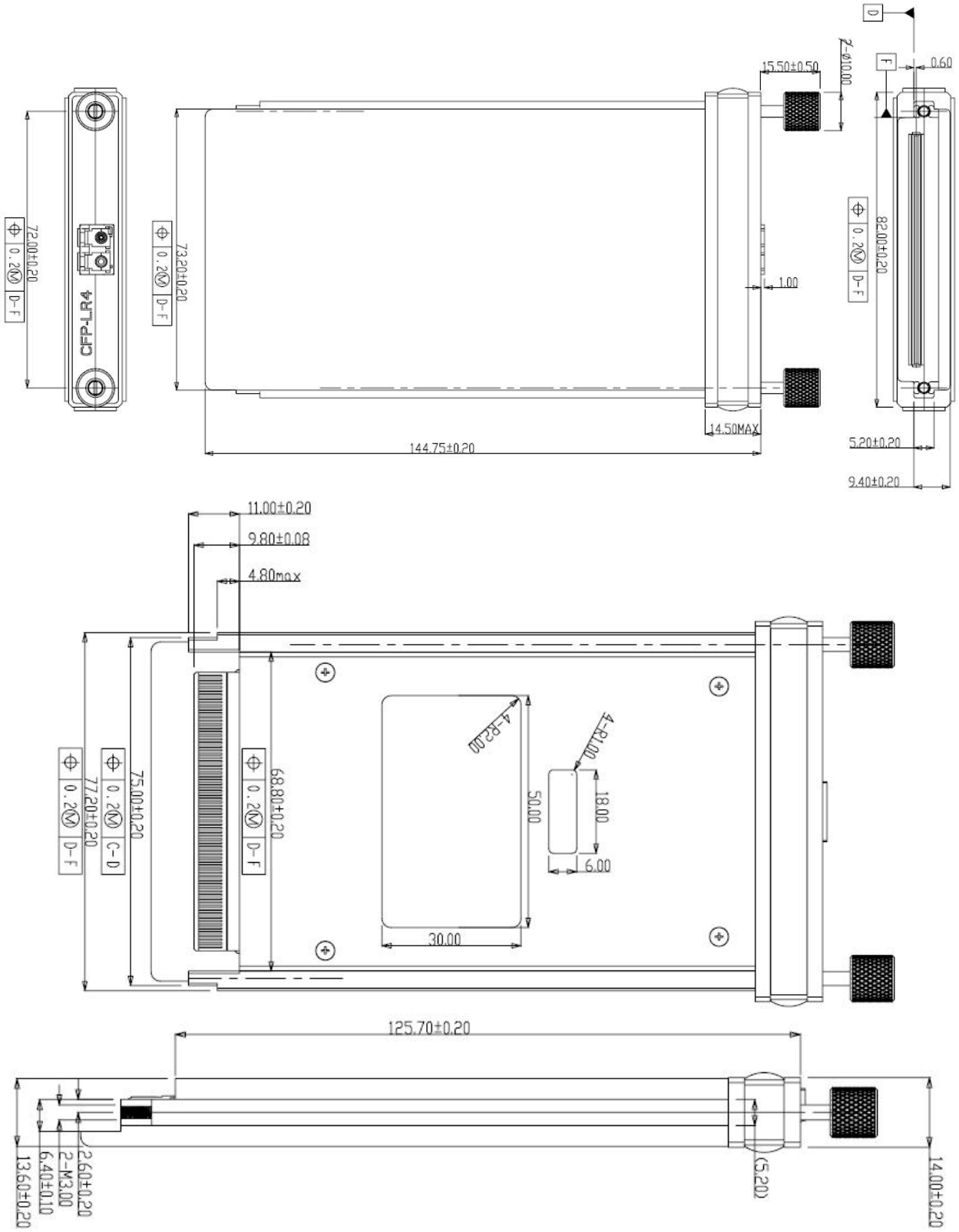


Pad Layout of the CFP module

CFP Optical Interface lanes and Assignment

Show the orientation of the single mode fiber facets of the optical connector.

Mechanical Dimensions



Unit: mm

Ordering information

Part Number	Product Description
GCF-S101-ZR-T-C-WA	100G CFP-DCO ZR, 112Gb/s, DWDM C-band Tunable, 120km, w/ EDFA, 22W
GCF-S101-ZR-T-C-NA	100G CFP-DCO ZR, 112Gb/s, DWDM C-band Tunable, 120km, w/o EDFA, 21W
GCF-S101-MR-T-C-WA	100G CFP-DCO MR, 112Gb/s, DWDM C-band Tunable, 600km, w/ EDFA, 23W
GCF-S101-MR-T-C-NA	100G CFP-DCO MR, 112Gb/s, DWDM C-band Tunable, 600km, w/o EDFA, 22W
GCF-S101-LH-T-C-WA	100G CFP-DCO LH, 112Gb/s, DWDM C-band Tunable, 1200km, w/ EDFA, 29W
GCF-S101-LH-T-C-NA	100G CFP-DCO LH, 112Gb/s, DWDM C-band Tunable, 1200km, w/o EDFA, 28W

Standards

1. Compliant with IEEE 802.3ba
2. Compliant with ITU-T G.709/Y.1331 Compliant with RoHS6
3. CFP-MSA-HW-Spec-rev1-40
4. CFP_MSA_MIS_V2p6r06a
5. CFP_MSA_Module-Dimensions_APRIL07-10
6. CFP_MSA_Host-Mechanical-drawings
7. OIF-MSA-100GLH-EM-02.1

Important Notice

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