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SFF-8679

Specification for

QSFP+ 4X Hardware and Electrical Specification

Revision 1.8 October 4, 2018

Secretariat: SFF TA TWG

Abstract: This specification defines the contact pads, the electrical, power supply, ESD and thermal characteristics of the pluggable QSFP+ module or cable plug.

There are multiple generations of QSFP+ that reference this specification:

SFF-8635 QSFP+ 4X 10 Gb/s Pluggable Transceiver Solution (QSFP10)
SFF-8685 QSFP+ 4X 14 Gb/s Pluggable Transceiver Solution (QSFP14)
SFF-8665 QSFP+ 4X 28 Gb/s Pluggable Transceiver Solution (QSFP+)

This specification supersedes the base electrical content of SFF-8436 QSFP+ 10Gb/s 4X Pluggable Transceiver.

This document provides a common specification for systems manufacturers, system integrators, and suppliers.

This draft specification is made available for public review, and written comments are solicited from readers. Comments received at http://www.snia.org/feedback will be considered for inclusion in future revisions of this specification.

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Change History

Rev 1.5:

- Moved referenced SFF specs to 2.1 Industry Documents and expanded the list.

Rev 1.6:

- Updated Figure 1 to show retimers.
- Removed two-wire interface timing diagram which is now in SFF-8636.
- Complete rewrite of power supply section to add support for Power Classes 5 to 7.
- Added section 8 "Timing Requirements".

Rev 1.7

- Editorial only, no technical changes.

Rev 1.8

- Converted to SNIA SFF template.
- Editorial updates throughout.
- Title changed to “Hardware and Electrical” to better reflect contents
- Updated abstract
- Updated editor contact information.
- Section 1 Scope – rewrote to better reflect content.
- Section 2 References – replaced several entries with updated document numbers and names.
- Section 2.3 Acronyms – deleted several unused entries and added several new ones based on content.
- Section 3 General Description – Rewrote most of this section to reflect updated content. Added several relevant applications to Table 3-1.
- Section 4 Compliance Testing – updated Figure 4-1 and corrected test point descriptions in Table 4-1.
- Section 5 Electrical Specification –
    - Updated Figure 5-1 and Table 5-1 to show the new dual-purpose signals LPMode/TxDis and IntL/RxLOSL on pads 31 and 28 respectively. Rewrote Note 2 of Table 5-1 for clarity.
    - Replaced “pin” by “pad” throughout
    - Replaced Figures 5-2 and 5-3 to better reflect current applications.
    - Extensive updates of Section 5.3 describing Low Speed Signals.
    - Updates to Table 5-2 to explain SCL and SDA electrical requirements and maximum pull-up resistor values for 400 kHz operation.
    - Significant revisions to text in 5.4 Low Speed Signal Electrical Specifications and 5.5 High Speed Signal Electrical Specifications.
    - Re-ordered and rewrote section 5.6 Power Supply Requirements including adding a new Power Class 8 with a maximum power limited only by the connector current rating.
- Section 6 Mechanical and Board Definition – cleaned up this section to reference the relevant documents instead of including non hardware/electrical features.
- Section 7 Environmental and Temperature – added a “custom” temperature class for modules that do not comply with any of the legacy case temperature ranges, e.g., hyperscale data center applications.
- Section 8 Timing Requirements
    - Major updates to Table 8-1 including re-writes of many entries in the “Conditions” column.
    - Changed limit for “Reset Init Assert Time” from a maximum of 2 us

to a minimum of 10 us.
    - Table 8-1: added new entries for “LPMode/TxDis mode change time”, “IntL/RxLOSL mode change time”, “RxLOSL Assert Time (Optional Fast Mode)”, and “RxLOSL Deassert Time (Optional Fast Mode)”.
    - Table 8-1: changed limit for “LPMode Assert Time” from 100 us to 100 ms.
    - Table 8-1: rewrote notes 1-5 and added new notes 6-7.
    - Table 8-2: changed maximum limits for “Rx Squelch Assert Time” and “Rx Squelch Deassert Time” from 80 us to 15 ms.
    - Table 8-2: added new parameters for “Tx Disable Assert Time (Optional Fast Mode)” and “Tx Disable Deassert Time (Optional Fast Mode)”.
    - Table 8-2: corrected text in descriptions of Tx Squelch assert & deassert.
    - Added section 8.3 and Table 8-3 with timing for ModSelL setup and hold times, plus time for aborted sequence – bus release.
- Appendix A two-wire interface timing – Added a copy of the two-wire interface timing diagram (Figure A-1), timing parameters (Table A-1) and non-volatile memory timing specifications (Table A-2).

Foreword

The development work on this specification was done by the SNIA SFF TWG, an industry group. Since its formation as the SFF Committee in August 1990, the membership has included a mix of companies which are leaders across the industry.

When 2 1/2" diameter disk drives were introduced, there was no commonality on external dimensions e.g. physical size, mounting locations, connector type, connector location, between vendors. The SFF Committee provided a forum for system integrators and vendors to define the form factor of disk drives.

During their definition, other activities were suggested because participants in SFF faced more challenges than the form factors. In November 1992, the charter was expanded to address any issues of general interest and concern to the storage industry. The SFF Committee became a forum for resolving industry issues that are either not addressed by the standards process or need an immediate solution.

In July 2016, the SFF Committee transitioned to SNIA (Storage Networking Industry Association), as a TA (Technology Affiliate) TWG (Technical Work Group).

Industry consensus is not a requirement to publish a specification because it is recognized that in an emerging product area, there is room for more than one approach. By making the documentation on competing proposals available, an integrator can examine the alternatives available and select the product that is felt to be most suitable.

SFF meets during the T10 (see http://www.incits.org/committees/t10) and T11 (see http://www.incits.org/committees/t11) weeks, and SSWGs (Specific Subject Working Groups) are held at the convenience of the participants.

Many of the specifications developed by SFF have either been incorporated into standards or adopted as standards by ANSI, EIA, JEDEC and SAE.

For those who wish to participate in the activities of the SFF TWG, the signup for membership can be found at: http://www.snia.org/sff/join

The complete list of SFF Specifications which have been completed or are currently being worked on by the SFF Committee can be found at: http://www.snia.org/sff/specifications

Suggestions for improvement of this specification will be welcome, they should be submitted to: http://www.snia.org/feedback

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1 Scope

This document specifies the electrical requirements for the QSFP10/14/28 pluggable 4-lane interfaces, hereafter referred to as QSFP+. The scope includes: electrical contacts for the host connector; status, control and management interface signals; power supply requirements; fiber positions for optical interfaces; ESD and thermal characteristics and color coding of pluggable QSFP+ modules and cables.

This specification supersedes and extends INF-8438 QSFP (Quad SFP) 4 Gb/s 4X Transceiver and SFF-8436 QSFP+ 10 Gb/s 4X Pluggable Transceiver by supporting higher transfer rates.

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2 References

2.1 Industry Documents

The following interface standards and specifications are relevant to this Specification.

- ANSI/TIA-568.3-D Optical Fiber Cabling And Components Standards
- ESD specifications EN61000-4-2, JEDEC JESD22-A114-B
- GR-253-CORE
- IEC 61754-7-1:2014 Fibre optic interconnecting devices and passive components- Fibre optic connector interfaces – Part 7-1: Type MPO connector family – One fibre row
- IEC 61754-20:2012 Fibre optic interconnecting devices and passive components- Fibre optic connector interfaces – Part 20: Type LC connector family
- IEEE Std 802.3
- IEEE P802.3cd
- INCITS 479-2011 Fibre Channel- Physical Interface -5 (FC-PI-5)
- INCITS 512-2015 Fibre Channel- Physical Interface -6 (FC-PI-6)
- INCITS 533-2016 Fibre Channel- Physical Interface -6P (FC-PI-6P)
- INCITS 543: Information technology – Fibre Channel – Physical Interfaces – 7 (FC-PI-7)
- INCITS 559: Information technology – Fibre Channel – Physical Interfaces – 7P (FC-PI-7P)
- InfiniBand Architecture Specification
- ISO/IEC 14776-154:2017 Information technology – Small computer system interface (SCSI) – Part 154: Serial Attached SCSI-3 (SAS-3)
- INCITS 534: Information technology - Serial Attached SCSI-4 (SAS-4)
- Telcordia GR-63-CORE, Issue 4, April 2012, NEBS™ Requirements: Physical Protection
- TIA-604-5 FOCIS 5 Fiber Optic Connector Intermateability Standard – Type MPO
- TIA-604-10 FOCIS 10B Fiber Optic Connector Intermateability Standard – Type LC

2.1.1 Relevant SFF Specifications

SFF specifications are available from http://www.snia.org/sff/specifications

- SFF-8024 SFF Committee Cross Reference to Industry Products
- SFF-8436 QSFP+ 10 Gb/s 4X Pluggable Transceiver – (EIA-964)
- INF-8438 QSFP (Quad Small Formfactor Pluggable) Transceiver
- SFF-8635 QSFP+ 10 Gb/s 4X Pluggable Transceiver Solution (QSFP10)
- SFF-8636 Management Interface for Cabled Environments
- SFF-8661 QSFP+ 28 Gb/s 4X Pluggable Module
- SFF-8662 QSFP+ 28 Gb/s 4X Connector (Style A)
- SFF-8663 QSFP+ 28 Gb/s Cage (Style A)
- SFF-8665 QSFP+ 28 Gb/s 4X Pluggable Transceiver Solution (QSFP28)
- SFF-8672 QSFP+ 28 Gb/s 4X Connector (Style B)
- SFF-8679 QSFP+ 4X Hardware and Electrical Specification
- SFF-8682 QSFP+ 4X Connector (Style B)
- SFF-8683 QSFP+ Cage
- SFF-8685 QSFP+ 14 Gb/s 4X Pluggable Transceiver Solution (QSFP14)

2.2 Conventions

The ISO convention of numbering is used i.e., the thousands and higher multiples are separated by a space and a period is used as the decimal point. This is equivalent to the English/American convention of a comma and a period.

American	French	ISO
0.6	0,6	0.6
1,000	1 000	1 000
1,323,462.9	1 323 462,9	1 323 462.9

2.3 Acronyms and Abbreviations

The following acronyms may be used in this specification.

ANSI	American National Standards Institute
ASIC	Application Specific Integrated Circuit
ATM	Asynchronous Transfer Mode
CDR	Clock and Data Recovery
CML	Current Mode Logic
CORE	Central Office Relay Equipment
CTLE	Continuous Time Linear Equalizer
DC	Direct Current
DDR	Double Data Rate
EDR	Extended Data Rate
EIA	Electronic Industries Alliance
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge
FC	Fibre Channel
FDR	Fourteen Gb/s Data Rate
Gb/s	Gigabits per second
GbE	Gigabit Ethernet
GFC	Gigabit Fibre Channel
HCB	Host Compliance Board
HDR	High Data Rate
IEC	International Electrotechnical Commission
IEEE	Institute for Electrical and Electronics Engineers
ISO	Organization for International Standards
ITU	International Telecommunications Union
JEDEC	Joint Electron Device Engineering Council
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor
LVTTL	Low Voltage Transistor Transistor Logic
MCB	Module Compliance Board
MPO	Multi-fiber Push On
NEBS	Network Equipment Building System
OC	Optical Carrier
OMA	Optical Modulation Amplitude
PCB	Printed Circuit Board
PI	Physical Interface
QDR	Quad Data Rate
QSFP	Quad SFP
Rx	Receiver
SAS	Serial Attached SCSI
SDH	Synchronous Digital Hierarchy
SDR	Single Data Rate
SerDes	Serializer-Deserializer
SFP	Small Formfactor Pluggable
SM	Single Mode
SONET	Synchronous Optical NETwork

STM	Synchronous Transfer Mode
TIA	Telecommunications Industry Association
TTL	Transistor-Transistor Logic
Tx	Transmitter

3 General Description

This specification covers the following items:

- Electrical specifications for QSFP+ modules including host connector contact assignments.
- Descriptions for data, control, status and management interface signals.
- Power supply requirements.
- Electrostatic discharge (ESD) tolerance requirements.
- Color coding and labeling.
- Fiber positions for optical interfaces.
- Environmental and thermal requirements (case temperatures).
- Timing requirements.

This specification may be compatible with the example optical and electrical specifications in Table 3-1.

TABLE 3-1 EXAMPLE USES FOR QSFP+

ITU-T Recommendation G.957	STM-1, STM-4, STM-16
Telcordia Technologies GR-253-CORE	OC-3, OC-12, OC-48, OC-192
IEEE Std. 802.3	10 GbE, 25 GbE, 40 GbE, 50 GbE, 100 GbE, 200 GbE
Infiniband Architecture Specification	SDR, DDR, QDR, FDR, EDR, HDR
Fibre Channel	8GFC, 16GFC, 32GFC, 128GFC
Serial Attached SCSI	SAS-3, SAS-4

The Application Reference Model in Figure 3-1 shows the high-speed data interface between an ASIC (SerDes) and the module. Only one lane of the interface is shown for simplicity. Either parallel MPO or duplex LC fiber connectors can be used for the optical interface.

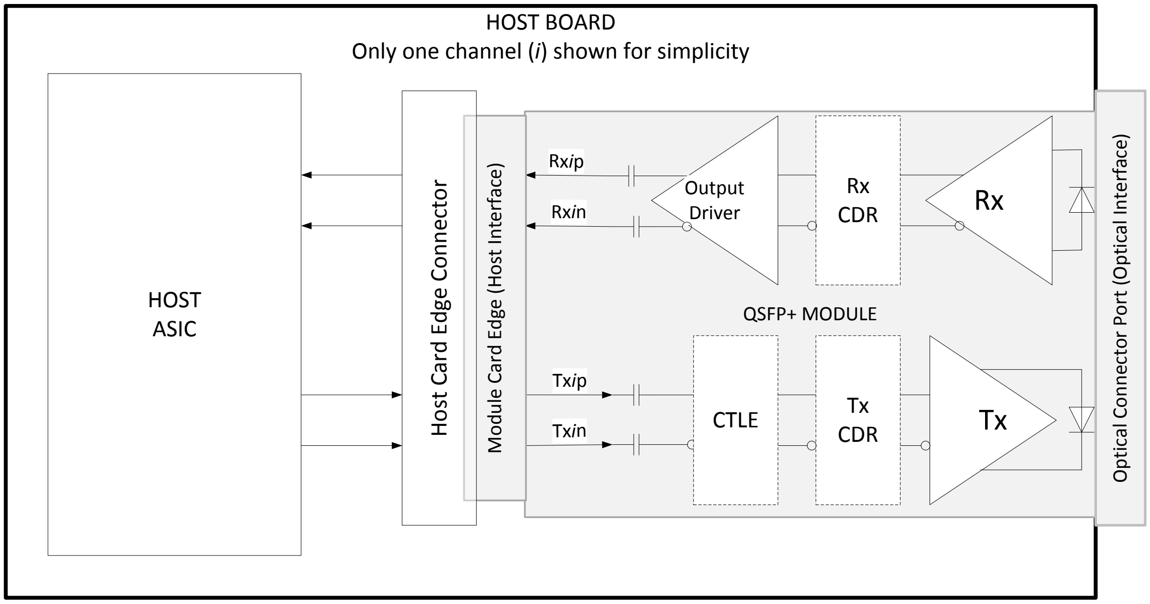

FIGURE 3-1 APPLICATION REFERENCE MODEL

4 Compliance boards and reference points

The module electrical interface test points are intended to be measured using compliance boards as shown in Figure 4-1. These compliance boards are intended to connect the module under test to test equipment for verification of compliance to the appropriate standard. The Module Compliance Board is used to test the module. The electrical parameters of the compliance boards should be specified by the appropriate standard. The Module Compliance Board and Host Compliance Board can be plugged together for calibration of compliance signals and to check the electrical parameters of the compliance boards. Reference points are described in Table 4-1.

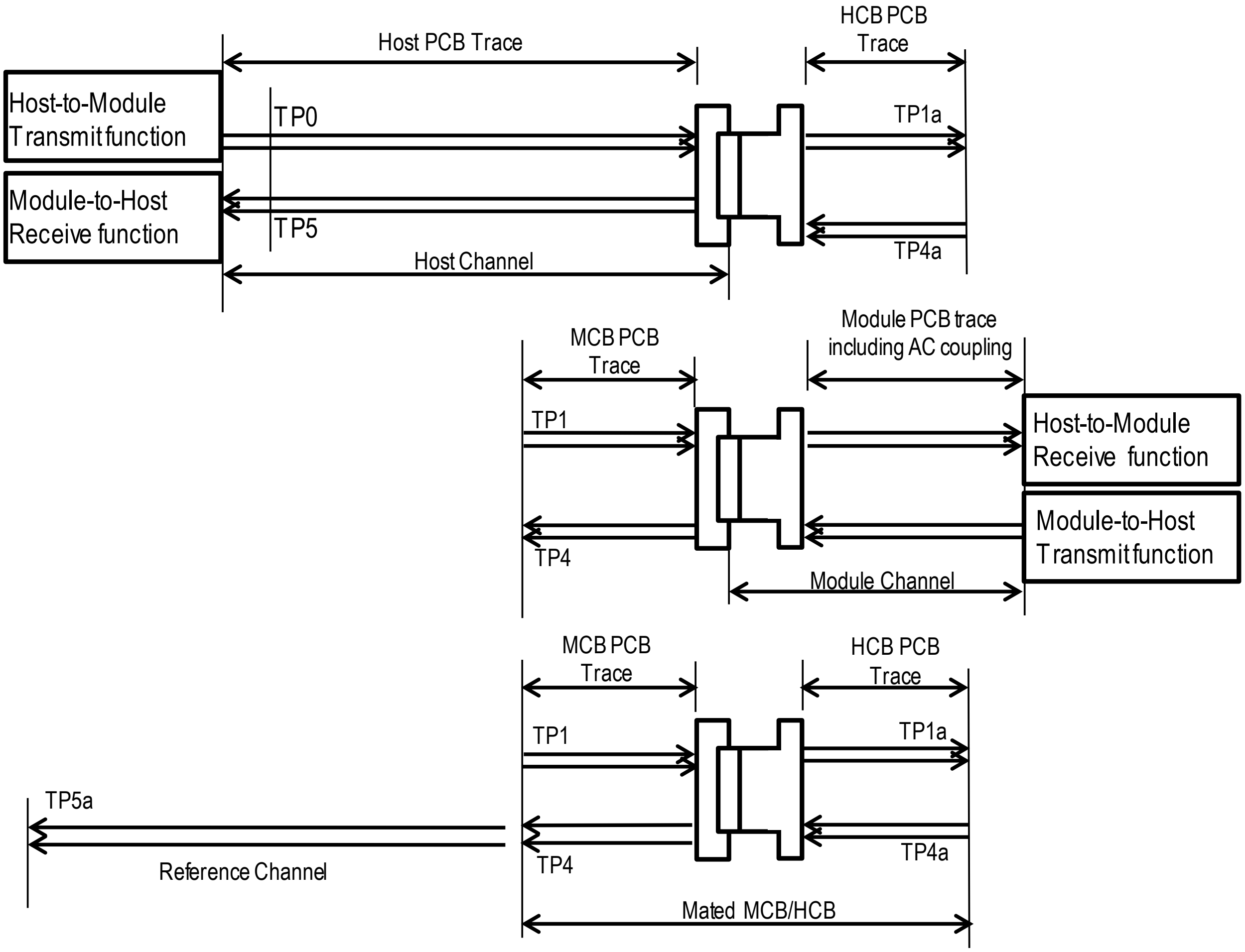

FIGURE 4-1 REFERENCE POINTS AND COMPLIANCE BOARDS

TABLE 4-1 REFERENCE POINTS

Reference point	Description
TP0	Host ASIC transmitter output at ASIC package contact.
TP1	Input to Module Compliance Board. Used to test module input.
TP1a	Host ASIC transmitter output through the host board and host card edge connector at the output of the Host Compliance Board. Also used to calibrate module input compliance signals.
TP4	Module output through the compliance board connectors at the output of the Module Compliance Board. Also used to calibrate host input compliance signals.
TP4a	Input to Host Compliance Board. Used to test host input.
TP5	Input to host ASIC
TP5a	Far end module output through a reference channel
Note: Individual standards may specify unique reference points	

5 Electrical Specification

This clause contains pad definition data for the module. The pad definition data is generic for high speed datacom applications such as Fibre Channel, Ethernet and SONET/ATM. Compliance Points for high-speed electrical measurements are defined in Table 4-1 and illustrated in Figure 4-1. Compliance points for all other electrical signals are at comparable points at the host card edge connector.

5.1 Electrical Connector

Figure 5-1 shows the signal symbols and pad numbering for the module edge connector. The diagram shows the module PCB edge as a top and bottom view, where bottom is nearer the host PCB. There are 38 pads intended for high speed signals, low speed signals, power and ground connections. Table 5-1 provides more information about each of the 38 pads.

The module contains a printed circuit board that mates with the electrical connector. The pads are designed for a sequenced mating:

Connected first, disconnected last:	- ground contacts
Connected second, disconnected second:	- power contacts
Connected third, disconnected first:	- signal contacts

For EMI protection the signals to the connector should be shut off when the module is absent. Standard board layout practices such as connections to Vcc and GND with vias, the use of short and equal-length differential signal lines, and the use of microstrip-lines and 50 Ω terminations are recommended. The chassis ground (case common) of the module should be isolated from the module's circuit ground, GND, to provide the equipment designer flexibility regarding connections between external electromagnetic interference shields and circuit ground, GND, of the module.

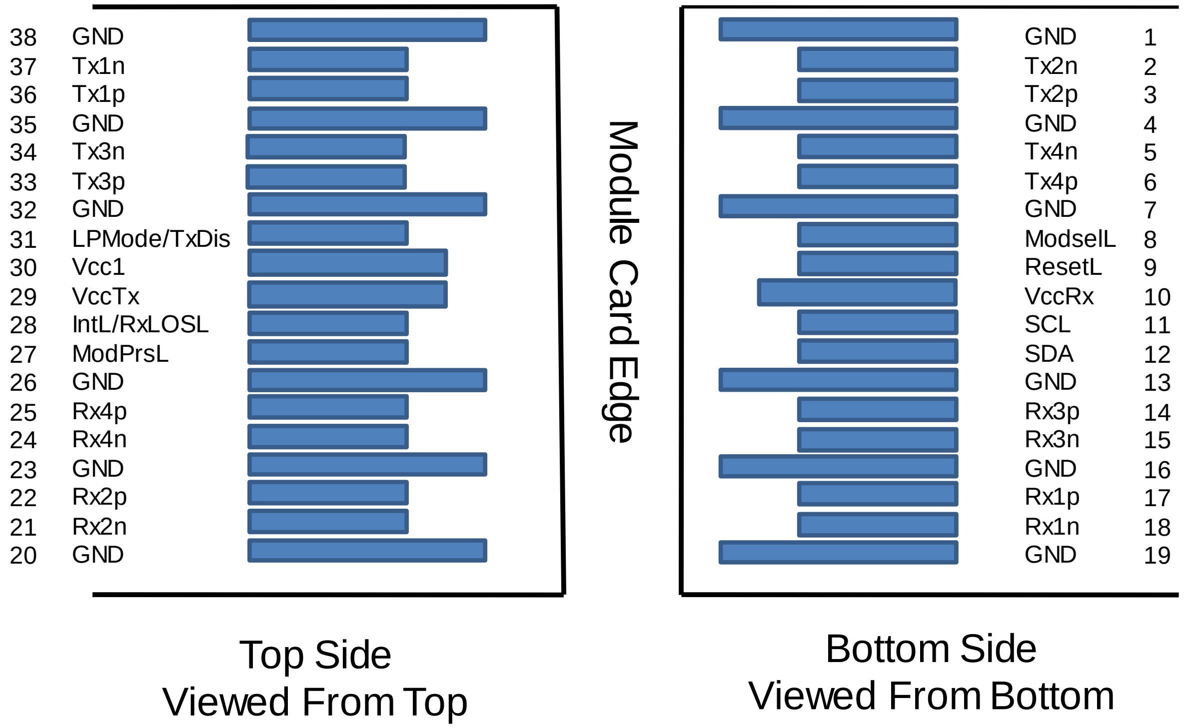

FIGURE 5-1 MODULE PAD LAYOUT

TABLE 5-1 PAD FUNCTION DEFINITION

Pad	Logic	Symbol	Description	Plug Seq-uence	Note
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		VccRx	+3.3V Power Supply Receiver	2	2
11	LVCMOS-I/O	SCL	Two-wire interface clock	3	
12	LVCMOS-I/O	SDA	Two-wire interface data	3	
13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL/RxLOSL	Interrupt. Optionally configurable as RxLOSL via the management interface (SFF-8636).	3	
29		VccTx	+3.3V Power supply transmitter	2	2
30		Vcc1	+3.3V Power supply	2	2
31	LVTTL-I	LPMode/TxDis	Low Power Mode. Optionally configurable as TxDis via the management interface (SFF-8636).	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1
Note 1: GND is the symbol for signal and supply (power) common for the module. All are common within the module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.					
Note 2: VccRx, Vcc1 and VccTx are applied concurrently and may be internally connected within the module in any combination. Vcc contacts in SFF-8662 and SFF-8672 each have a steady state current rating of 1 A.					

5.2 QSFP Example Circuits

Figure 5-2 and Figure 5-3 provide example host board schematics for an optical QSFP+ module and for a QSFP+ copper cable plug respectively. Optical modules may have CDRs and equalizers in the module depending on the application.

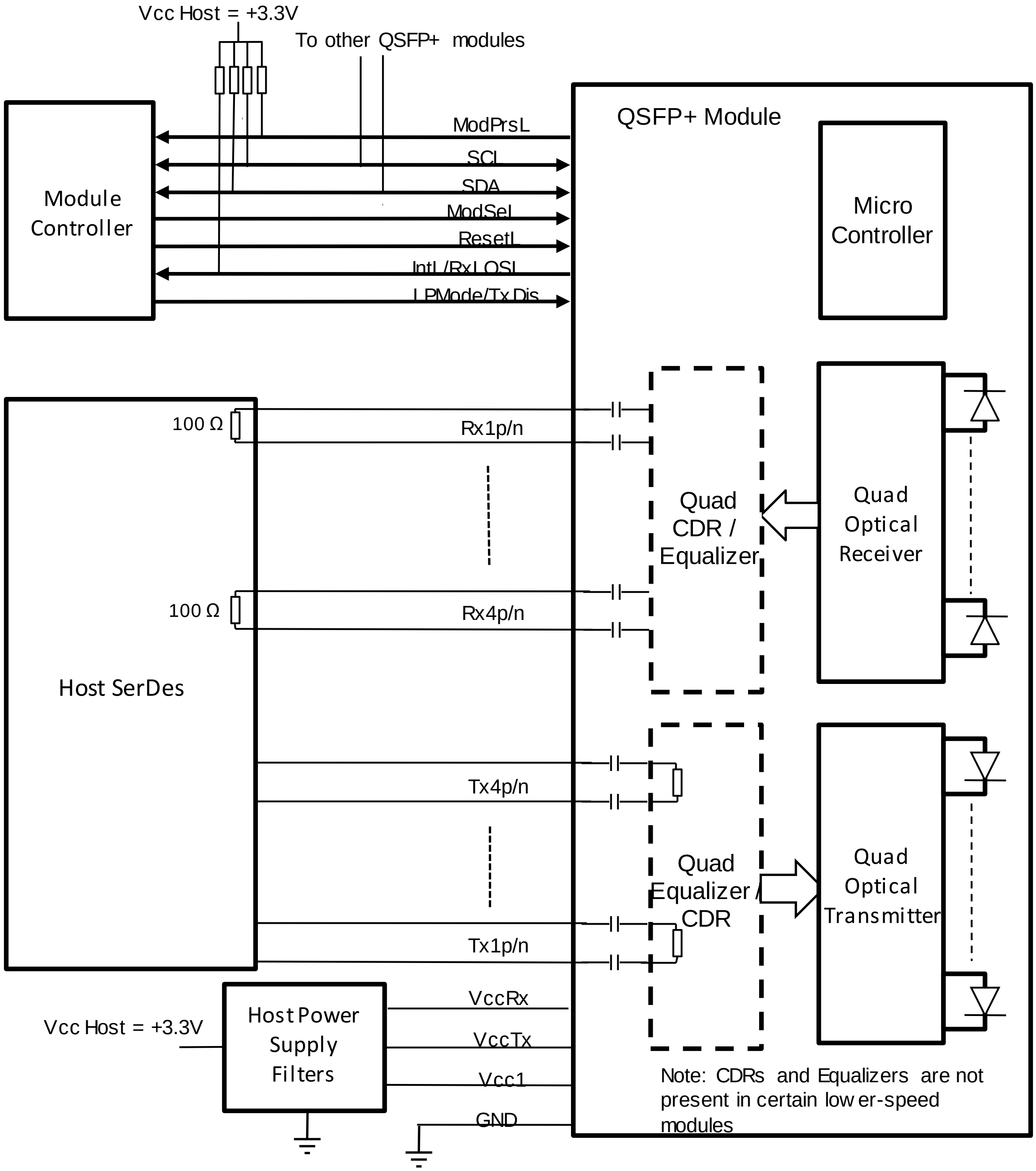

FIGURE 5-2 EXAMPLE: HOST BOARD SCHEMATIC FOR OPTICAL MODULES

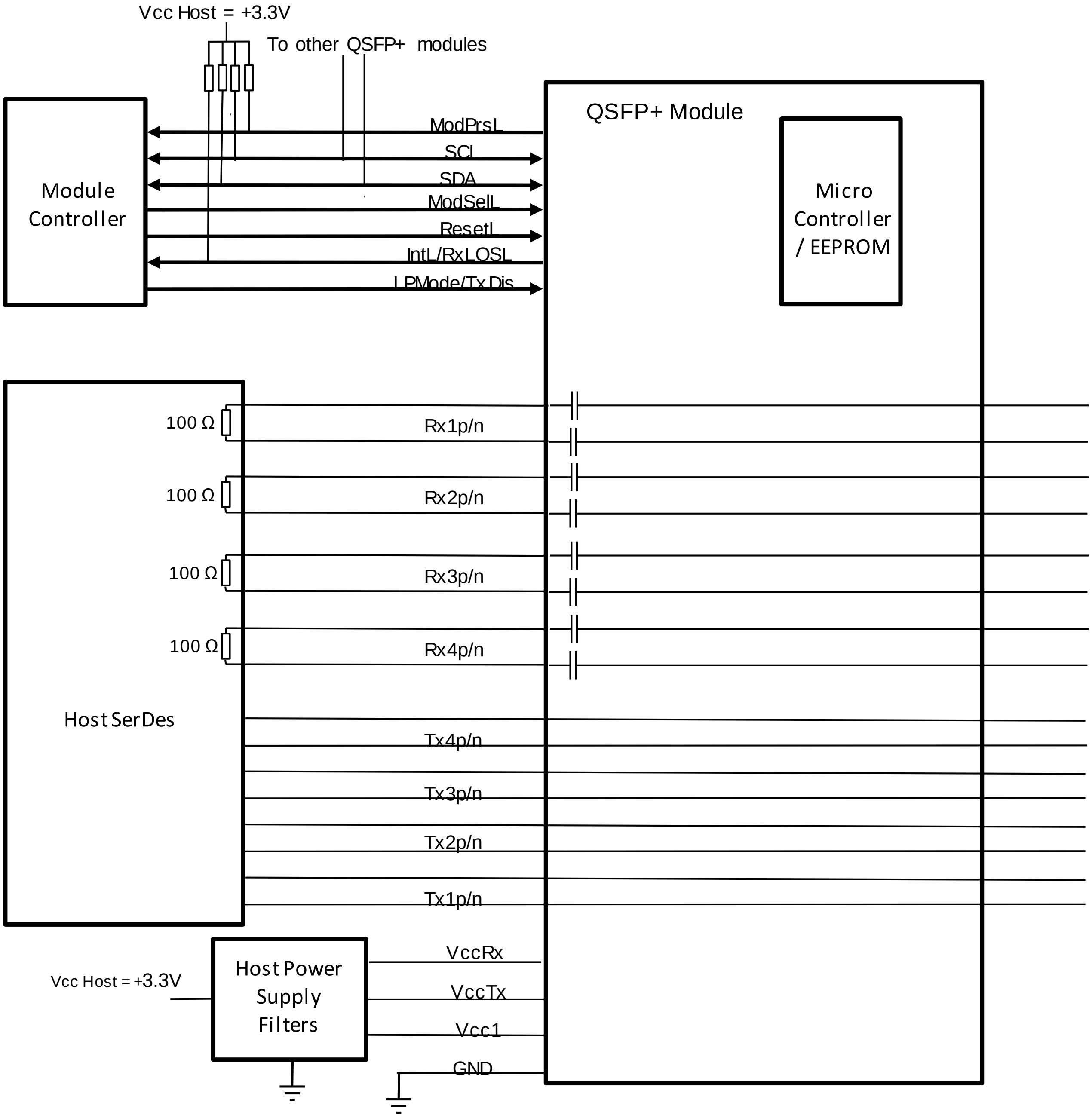

FIGURE 5-3 EXAMPLE: HOST BOARD SCHEMATIC FOR PASSIVE COPPER CABLES

5.3 Low Speed Signal Descriptions

In addition to the two-wire interface the module has the following low speed signals for control and status:

ModSelL
ResetL
LPMode/TxDis
ModPrsL
IntL/RxLOSL

The behavior of these signals is given in 5.3.1 to 5.3.5, the electrical specifications are in 5.4.1, and timing requirements are in 5.4.2 and 8. Timing requirements for the two-wire interface are in Appendix A.

5.3.1 ModSelL

ModSelL is an input signal. When held low by the host, the module responds to two-wire serial communication commands. The ModSelL signal allows the use of multiple modules on a single two-wire interface. When ModSelL is high, the module shall not respond to or acknowledge any two-wire interface communication from the host. The ModSelL signal input node shall be pulled towards Vcc in the module.

In order to avoid conflicts, the host system shall not attempt two-wire interface communications within the ModSelL de-assert time after any modules are deselected. Similarly, the host shall wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-assertion periods of different modules may overlap as long as the above timing requirements are met.

5.3.2 ResetL

The ResetL signal shall be pulled towards Vcc in the module. A low level on ResetL for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level of the ResetL pad is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of reset interrupt by asserting "low" on the IntL/RxLOSL signal (see SFF-8636 for details). However, on power up (including hot insertion) the module should post this completion of reset interrupt without the host pulling ResetL low.

5.3.3 LPMode/TxDis

LPMode/TxDis is a dual-mode input signal from the host operating with active high logic. It shall be pulled towards Vcc in the module. At power-up or after ResetL is deasserted LPMode/TxDis behaves as LPMode. If supported, LPMode/TxDis can be configured as TxDis using the two-wire interface except during the execution of a reset. TxDis provides an optional fast mode, see definition in SFF-8636.

When LPMode/TxDis is configured as LPMode, the module behaves as though TxDis=0. By using the LPMode signal and a combination of the Power_override, Power_set and High_Power_Class_Enable software control bits (SFF-8636, Address A0h, Byte 93 bits 0,1,2), the host controls how much power a module can consume. See section 5.6 for more details on the power supply specifications.

When LPMode/TxDis is configured as TxDis, the module behaves as though LPMode=0. In this mode LPMode/TxDis when set to 1 or 0 disables or enables all optical transmitters within the times specified in Table 8-2.

Changing LPMode/TxDis mode from LPMode to TxDis when the LPMode/TxDis state is high disables all optical transmitters. If the module was in low power mode, then the module transitions out of low power mode at the same time. If the module is already in high power state (Power Override control bits) with transmitters already enabled, the module shall disable all optical transmitters.

Changing the LPMode/TxDis mode from LPMode to TxDis when the LPMode/TxDis state is low, simply changes the behavior of the mode of LPMode/TxDis. The behavior of the module depends on the Power Override control bits.

Timing requirements for LPMode/TxDis mode changes are found in Table 8-1.

Note that the “soft” functions of TxDis, LPMode, IntL and RxLOSL allow the host to poll or set these values over the two-wire interface as an alternative to monitoring/setting signal values. Asserting either the “hard pin” or “soft bit” (or both) for TxDis or LPMode results in that function being asserted.

5.3.4 ModPrsL

ModPrsL is pulled up towards Vcc_Host on the host board and pulled towards ground in the module. ModPrsL is pulled low when inserted and released to high when it is physically absent from the host connector.

5.3.5 IntL/RxLOSL

IntL/RxLOSL is a dual-mode active-low, open-collector output signal from the module. It shall be pulled up towards Vcc on the host board. At power-up or after ResetL is released to high, IntL/RxLOSL is configured as IntL. If supported, IntL/RxLOSL can be optionally programmed as RxLOSL using the two-wire interface except during the execution of a reset. See definition in SFF-8636. Rx LOS and RxLOSL timings, including an optional fast mode, are given in 8.1.

If IntL/RxLOSL is configured as IntL, a low indicates a possible module operational fault or a module condition that sets an unmasked flag as defined in SFF-8636. The source of the IntL “low” can be read, cleared or masked using the two-wire interface. If the interrupt was after a module reset and SFF-8636, Page 00h, Byte 2, bit 0 (Data_Not_Ready bit) is 0, then the module releases IntL to high after the host has read the Data_Not_Ready bit. For all other interrupt causes, the module releases IntL to high after the host has read the flag associated with the cause of the interrupt.

If IntL/RxLOSL is configured as RxLOSL, a low indicates that there is a loss of received optical power on at least one lane. “high” indicates that there is no loss of received optical power. Rx LOS and RxLOSL timings, including an optional fast mode, are given in Table 8-2. The actual condition of loss of optical receive power is specified by other governing documents, as the alarm threshold level is application specific. The module shall pull RxLOSL to low if any lane in a multiple lane module or cable has a LOS condition and shall release RxLOSL to high only if no lane has a LOS condition.

Timing requirements for IntL/RxLOSL mode change are found in Table 8-1. If the module has no interrupt flags asserted (IntL/RxLOSL is high), there should be no change in IntL/RxLOSL states after the mode change.

5.4 Low Speed Signal Electrical Specifications

5.4.1 Low Speed Signaling

Low speed signaling other than SCL and SDA is based on Low Voltage TTL (LVTTL) operating at Vcc. Vcc refers to the generic supply voltages of VccTx, VccRx, Vcc_host or Vcc1. Hosts shall use a pull-up resistor connected to Vcc_host on each of the two-wire interface SCL (clock) and SDA (data), and all low speed status outputs.

The SCL and SDA is a hot plug interface that may support a bus topology. During module insertion or removal, the module may implement a pre-charge circuit which prevents corrupting data transfers from other modules that are already using the bus.

Compliance with Table 5-2 provides compatibility between host bus masters and the two-wire interface.

TABLE 5-2 LOW SPEED ELECTRICAL SPECIFICATIONS

Parameter	Symbol	Min	Max	Unit	Notes/Conditions
SCL and SDA	VOL	0	0.4	V	IOL(max)=3.0 mA
	VOH	Vcc-0.5	Vcc+0.3	V	
SCL and SDA	VIL	-0.3	Vcc*0.3	V	
	VIH	Vcc*0.7	Vcc + 0.5	V	
Capacitance on SCL and SDA I/O contact.	Ci		14	pF	Looking into the module SCL and SDA contacts.
Total bus capacitive load for SCL and SDA for up to 400 kHz SCL rate (includes capacitance of all elements on the bus).	Cb		100	pF	3.0 kΩ pullup resistor
			200	pF	1.6 kΩ pullup resistor
LPMode/TxDis, ResetL and ModSelL	VIL	-0.3	0.8	V	
	VIH	2	Vcc+0.3	V	
	Iin	-365	125	μA	0 V ≤ Vin ≤ Vcc
ModPrsL and IntL/RxLOSL	VOL	0	0.4	V	IOL=2.0mA
	VOH	Vcc-0.5	Vcc+0.3	V	

Notes: Positive values indicate current flowing into the module. See Appendix A for management interface (SCL, SDA) timing information.

5.4.2 Low Speed Signal Timing

Timing for SCL and SDA is defined in a management interface document, SFF-8636 and is duplicated in Appendix A for convenience. Timing of the hardware control functions and ModSelL are specified in section 8.

5.5 High Speed Signal Electrical Specifications

For detailed high-speed requirements see the appropriate specification, e.g. IEEE Std 802.3, Fibre Channel, OIF-CEI or InfiniBand. Partial or complete squelch requirements may be provided in the appropriate specification. Where the relevant specification does not provide a requirement or a recommendation, the following subclauses shall apply.

5.5.1 Rx*i*p and Rx*i*n

Rx*i*p and Rx*i*n are module receiver data outputs. They are AC-coupled 100 Ω differential lines that should be terminated with 100 Ω differentially at the host

ASIC (SerDes). The AC coupling is inside the module and not required on the Host board.

Due to the possibility of insertion of legacy QSFP and QSFP+ modules into a host designed for higher speed operation, it is recommended that the damage threshold of the host input be at least 1600 mV peak to peak differential.

Output squelch for loss of optical input signal, hereafter Rx Squelch, is required and shall function as follows. In the event that the optical signal on any lane becomes less than or equal to the level required to assert LOS, then the receiver data output for that lane shall be squelched or disabled and the associated RxLOS flag set. In the squelched or disabled state output impedance levels are maintained while the differential voltage swing shall be less than 50 mVpp or the value in the relevant standard.

In normal operation the default case has Rx Squelch active. Rx Squelch can be deactivated using Rx Squelch Disable through the two-wire interface. Rx Squelch Disable is an optional function. For specific details refer to SFF-8636.

5.5.2 Tx*i*p and Tx*i*n

Tx*i*p and Tx*i*n are module transmitter data inputs. They are AC-coupled 100 Ω differential lines with 100 Ω differential terminations inside the module. The AC coupling is inside the module and not required on the Host board.

Due to the possibility of insertion of modules into a host designed for lower speed operation, the damage threshold of the module input shall be at least 1600 mV peak to peak differential.

Output squelch, hereafter Tx Squelch, for loss of input signal, hereafter Tx LOS, is an optional function. Where implemented it shall function as follows. In the event that the input signal becomes less than 50 mVpp or the value in the relevant standard, then the transmitter optical output for that lane shall be squelched or disabled and the associated TxLOS flag set.

Where squelched, the transmitter OMA shall be less than or equal to -26 dBm and when disabled the transmitter power shall be less than or equal to -30 dBm or the value(s) defined by the relevant standard. For applications, e.g. Ethernet, where the transmitter off condition is defined in terms of average power, disabling the transmitter is recommended and for applications, e.g. InfiniBand, where the transmitter off condition is defined in terms of OMA, squelching the transmitter is recommended.

In module operation, where Tx Squelch is implemented, the default case has Tx Squelch active. Tx Squelch can be deactivated using Tx Squelch Disable through the two-wire interface. Tx Squelch Disable is an optional function. For specific details refer to SFF-8636.

5.6 Power Supply Requirements

A host board together with the QSFP+ module(s) forms an integrated power system. The host supplies stable power to the module. The module limits electrical noise coupled back into the host system and limits inrush charge/current during hot plug insertion.

The circuit card in a QSFP+ module has three designated power pads, designated VccTx, VccRx and Vcc1. When the QSFP+ module is "hot plugged" into a connector with power already present, the three pads have power applied concurrently. The module is responsible for limiting the inrush current surge from the reference power supply filtering circuit during a hot plug event. The host power supply may supply up to the maximum inrush current limits during a hot plug event without causing disturbance to other modules and components on the same power supply.

All specifications shall be met at the maximum power supply current. No power sequencing of the power supply is required of the host system. The module sequences the contacts in the order of ground, supply and signals during insertion.

5.6.1 Host Board Power Supply Filtering

The host board should use a power supply filtering network equivalent to that shown in Figure 5-4.

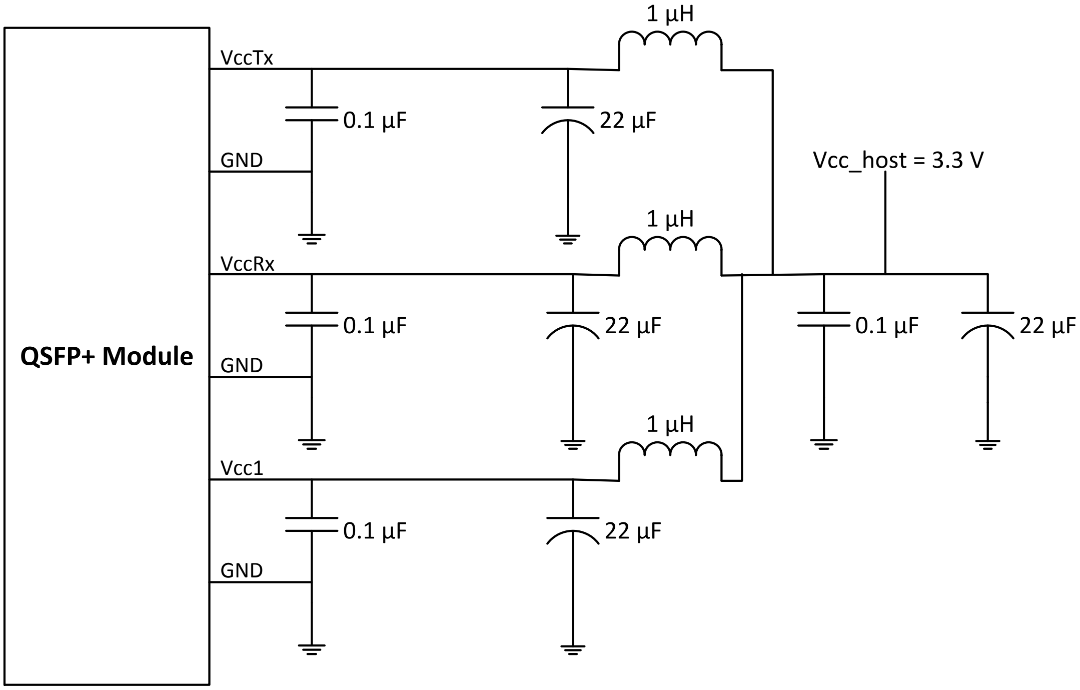

FIGURE 5-4 RECOMMENDED HOST BOARD POWER SUPPLY FILTERING

Any voltage drop across a filter network on the host is counted against the host DC set point accuracy specification. Inductors with DC resistance of less than 0.1 Ω should be used in order to maintain the required voltage at the host edge card connector. It is recommended that the 22 uF capacitors each have an equivalent series resistance of 0.22 Ω.

The specification of the host power supply filtering network is beyond the scope of this specification, particularly because of the wide range of QSFP+ module Power Classes. An example current waveform into a host filter, labeled I1 in Figure 5-5 is plotted in Figure 5-6. Each power connection has a supply filter for reducing high frequency noise and ripple from host-to-module. During a hot-plug event, the filter network limits any voltage drop on the host supply so that neighboring modules sharing the same supply stay within their specified supply voltage limits.

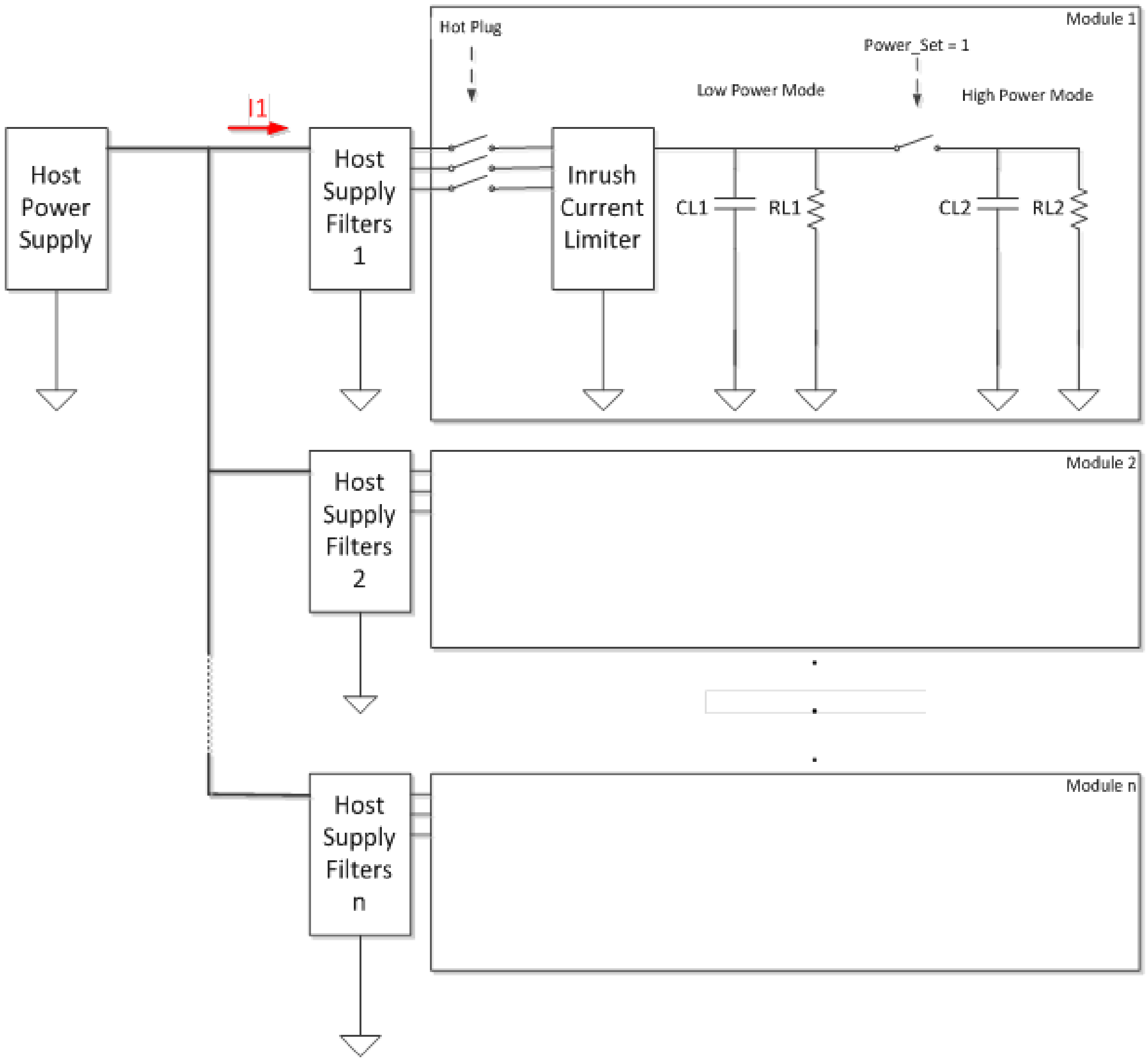

FIGURE 5-5 EXAMPLE: SCHEMATIC OF MULTIPLE QSFP+ POWER SUPPLY ARRANGEMENT

5.6.2 Power Classes and Maximum Power Consumption

Since different classes of modules exist with pre-defined maximum power consumption limits, it is necessary to avoid exceeding the host power supply limits and cooling capacity when a module is inserted into a host designed to use only lower power modules. It is recommended that the host, through the management interface, identify the power consumption class of the module before allowing the module to go into High Power Mode.

QSFP+ modules are categorized into several Power Classes as listed in Table 5-3. Power Classes are advertised in SFF-8636, Page 00h, Byte 129. The maximum power consumption may be advertised in SFF-8636, Page 00h, Byte 107.

TABLE 5-3 QSFP+ MODULE POWER CLASSES

Power Class	Maximum power consumption per module (W)
1	1.5
2	2.0
3	2.5
4	3.5
5	4.0
6	4.5
7	5.0
8	10.0 (Note)

Note: For power class 8, maximum power consumption is declared by the module in SFF-8636, Page 00h, Byte 107.

In order to avoid exceeding the host system power capacity and thermal management, upon hot-plug, power cycle or reset, all QSFP+ modules shall power up as if they were Power Class 1, designated as "Low Power Mode". QSFP+ modules that are Power Class 1 are fully functional after initialization and remain in Low Power Mode during operation. All other QSFP+ modules reach fully functional operation only after the host system enables High Power Mode".

High Power Mode is defined as the Power Class advertised in SFF-8636, Page 00h, Byte 129 and is enabled by the host if the host can supply sufficient power to the module. The host system controls whether a particular Power Class is enabled using the LPMode input pad and/or by writing to four control bits in SFF-8636, Page 00h, Byte 93. The management interface specification, SFF-8636 provides complete details but for explanation of power supply control, the bits are listed in Table 5-4.

TABLE 5-4 POWER MODE CONTROL BITS IN SFF-8636, PAGE 00H, BYTE 93)

Bit	Name	Description
7-4	Reserved	
3	High Power Class Enable (Class 8)	When set to 1 enables Power Class 8 if listed in Byte 129. When cleared to 0, modules with Power Class 8 shall dissipate less than the power specified by bit 2, but are not required to be fully functional. Refer to Table 5-5. Default=0.
2	High_Power_Class_Enable (Classes 5-7)	When set to 1 enables Power Classes 5 to 7 if listed in Byte 129. When cleared to 0, modules with Power Classes 5 to 8 shall dissipate less than 3.5 W, but are not required to be fully functional. Default=0.
1	Power_set	Power set to Low Power Mode (Power Class 1). Default=0.
0	Power_override	Override of LPMode/TxDis pad state to allow power mode setting by software.

Note: Power Class 8 is managed by SFF-8636 rev 3.0 or higher.

A truth table showing the allowed Power Classes is shown in Table 5-5.

TABLE 5-5 POWER MODE TRUTH TABLE

Power_override Byte 93 bit 0	Power_set Byte 93 bit 1	High_Power_ Class_Enable (Class 5-7) Byte 93 bit 2	High_Power_ Class_Enable (Class 8) Byte 93 bit 3	LPMode/TxDis pad state	Module Power Classes Enabled
Power consumption controlled by LPMode/TxDis pad state					
0	X	0	0	1	1
0	X	0	0	0	1 to 4
0	X	1	0	1	1
0	X	1	0	0	1 to 7
0	X	X	1	1	1
0	X	1	1	0	1 to 8
0	X	0	1	0	8
Power consumption controlled by Power_set bit					
1	1	0	0	X	1
1	0	0	0	X	1 to 4
1	1	1	0	X	1
1	0	1	0	X	1 to 7
1	1	X	1	X	1
1	0	1	1	X	1 to 8
1	0	0	1	X	8

5.6.3 Module Power Supply Specification

Module power supply specifications are given in Table 5-6.

QSFP+ modules operate from the host supplied voltage at the three power pads. To protect the host and system operation, each QSFP+ module during hot plug and normal operation shall follow the requirements listed in Table 5-6 and illustrated in Figure 5-6.

The test configuration for measuring the supply current is a module power compliance board with reference power supply filters, similar to the circuit shown in Appendix D and Figure 56 of SFF-8431. The current limits in Table 5-6 refer to the sum of the three currents, e.g. the equivalent of the current through the 0.1 Ω sense resistor in Figure 56 of SFF-8431.

An example current waveform into a host filter, labeled I1 in Figure 5-5 is plotted in Figure 5-6. This figure also shows the timing of the initial module turn-on in Low Power Mode, and the later transition to full power mode after the host system has enabled it via the two-wire interface.

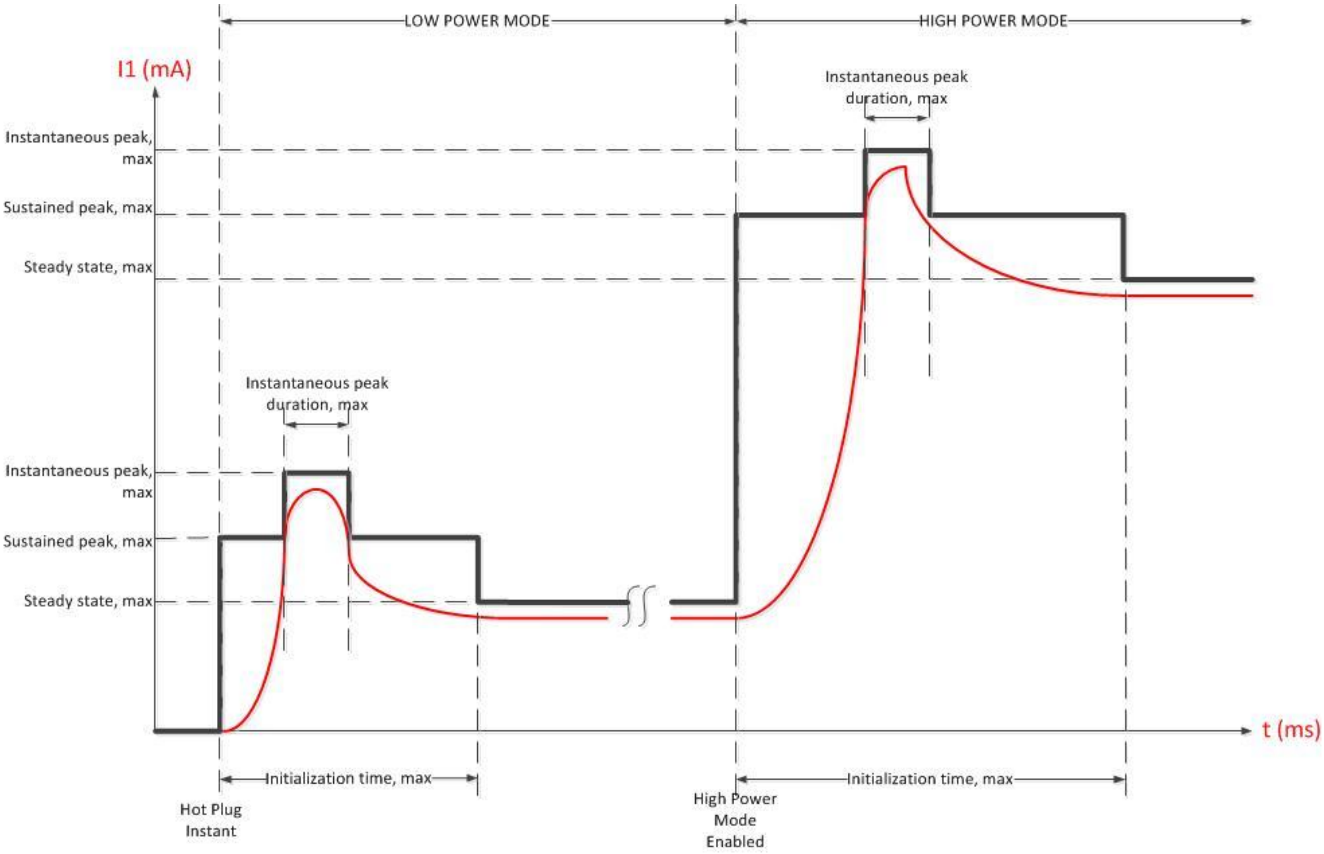

FIGURE 5-6 QSFP+ INRUSH CURRENT TIMING

TABLE 5-6 QSFP+ MODULE POWER SUPPLY SPECIFICATION

Parameter	Symbol	Min	Nom	Max	Unit
Power supply voltages VccTx, VccRx and Vcc1 including ripple, droop and noise below 100 kHz (Note 1)		3.135	3.3	3.465	V
Host RMS noise output 10 Hz to 10 MHz				25	mV
Module RMS noise output 10 Hz to 10 MHz (Note 2)				15	mV
Module power supply noise tolerance 10 Hz to 10 MHz (peak-to-peak)	PSNR_Mod			66	mV
Module inrush - instantaneous peak duration	T_ip	-	-	50	µs
Module inrush - initialization time	T_init	-	-	500	ms
Power Class 1 module and Low Power Mode for other modules					
Power consumption	P_1	-	-	1.5	W
Instantaneous peak current at hot plug	Icc_ip_1	-	-	600	mA
Sustained peak current at hot plug	Icc_sp_1	-	-	495	mA
Steady state current (Note 3)	Icc_1	-	-	432.9	mA
High Power Mode Power Class 2 module					
Power consumption	P_2	-	-	2	W
Instantaneous peak current at hot plug	Icc_ip_2	-	-	800	mA
Sustained peak current at hot plug	Icc_sp_2	-	-	660	mA
Steady state current (Note 3)	Icc_2	-	-	577.2	mA
High Power Mode Power Class 3 module					
Power consumption	P_3	-	-	2.5	W
Instantaneous peak current at hot plug	Icc_ip_3	-	-	1000	mA
Sustained peak current at hot plug	Icc_sp_3	-	-	825	mA
Steady state current (Note 3)	Icc_3	-	-	721.5	mA
High Power Mode Power Class 4 module					
Power consumption	P_4	-	-	3.5	W
Instantaneous peak current at hot plug	Icc_ip_4	-	-	1400	mA
Sustained peak current at hot plug	Icc_sp_4	-	-	1155	mA
Steady state current (Note 3)	Icc_4	-	-	1010.1	mA
High Power Mode Power Class 5 module					
Power consumption	P_5	-	-	4	W
Instantaneous peak current at hot plug	Icc_ip_5	-	-	1600	mA
Sustained peak current at hot plug	Icc_sp_5	-	-	1320	mA
Steady state current (Note 3)	Icc_5	-	-	1154.4	mA
High Power Mode Power Class 6 module					
Power consumption	P_6	-	-	4.5	W
Instantaneous peak current at hot plug	Icc_ip_6	-	-	1800	mA
Sustained peak current at hot plug	Icc_sp_6	-	-	1485	mA
Steady state current (Note 3)	Icc_6	-	-	1298.7	mA
High Power Mode Power Class 7 module					
Power consumption	P_7	-	-	5	W
Instantaneous peak current at hot plug	Icc_ip_7	-	-	2000	mA
Sustained peak current at hot plug	Icc_sp_7	-	-	1650	mA
Steady state current (Note 3)	Icc_7	-	-	1443.0	mA
High Power Mode Power Class 8 module					
Power consumption (Note 4)	P_8	-	-	10	W
Instantaneous peak current at hot plug	Icc_ip_8	-	-	P_8/2.5	A
Sustained peak current at hot plug	Icc_sp_8	-	-	P_8/3.03	A
Steady state current (Note 3)	Icc_8	-	-	3	A
Note 1: Measured at VccTx, VccRx and Vcc1. Note 2: See 5.6.5 Note 3: The module must stay within its advertised power class for all supply voltages. Note 4: Maximum power consumption is advertised in SFF-8636, Page 00h, Byte 107.					

5.6.4 Host Board Power Supply Noise Output

The host shall generate an effective weighted integrated spectrum RMS noise less than the value in Table 5-6 when tested by the methods of SFF-8431, section D.17.1. The resistive load for the test needs to be tailored for the QSFP power class and may be implemented using constant current sink circuits attached to each host supply filter output.

5.6.5 Module Power Supply Noise Output

The QSFP+ module shall generate less than the value in Table 5-6 when tested by the methods of SFF-8431, section D.17.2. The test fixture source resistor should be scaled by the ratio: (1.5W / maximum module power consumption), where maximum module power consumption is either the maximum of the advertised power class, or the advertised maximum power.

5.6.6 Module Power Supply Noise Tolerance

The QSFP+ module shall meet all requirements and remain fully operational in the presence of a sinusoidal tolerance signal of amplitude given by Table 5-6, swept from 10 Hz to 10 MHz according to the methods of SFF-8431, section D.17.3. This emulates the worst-case noise output of the host. The source resistance for the power supply and sine wave generator may need to be reduced from 0.5 Ω to a lower value for high powered modules.

5.7 ESD

Where ESD performance is not otherwise specified, e.g. in the InfiniBand specification, the module shall meet ESD requirements given in EN61000-4-2, criterion B test specification when installed in a properly grounded cage and chassis. The units are subjected to 15 kV air discharges during operation and 8 kV direct contact discharges to the case.

The module and host shall withstand 1000 V electrostatic discharge based on Human Body Model per JEDEC JESD22-A114-B for all pins.

6 Mechanical and Board Definition

6.1 Mechanical general

The overall module defined in this clause is illustrated in Figure 6-1. The optical interface is described in section 6.3. Several cage-to-bezel options are possible. Both metal spring finger and elastomeric EMI solutions are permitted. Heat sink/clip thermal designs are not defined by this specification; however, general designs are described in SFF-8663 and SFF-8683.

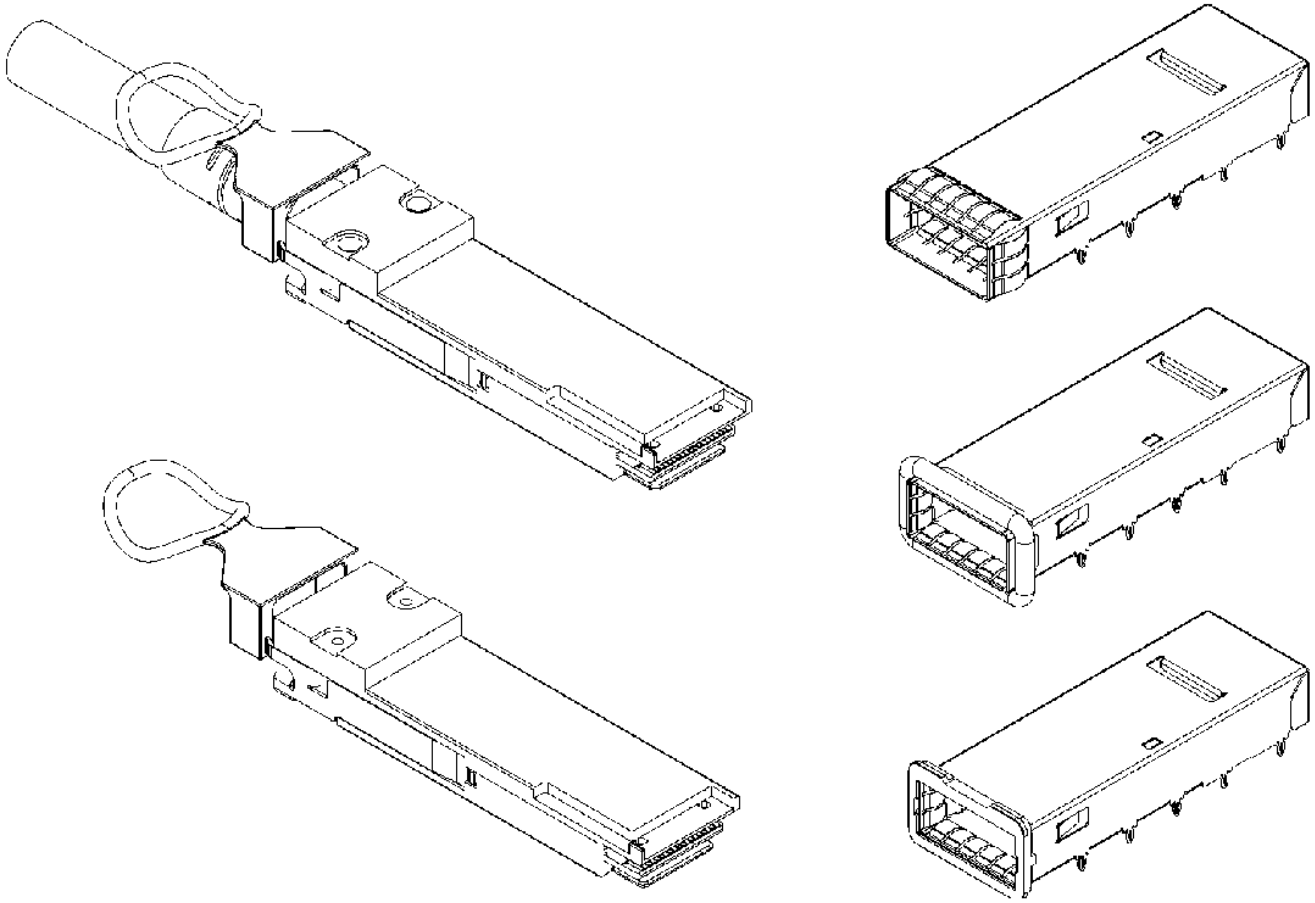

FIGURE 6-1 PLUGGABLE MODULE AND CABLE PLUG RENDERING

6.2 Color Coding and Labeling of Modules

An exposed feature of the module (a feature or surface visible when the module is fully inserted in the host) shall be color coded. Unless industry specifications apply, the following colors should be used.

Beige for 850 nm
Blue for 1310 nm
White for 1550 nm

Each module shall be clearly labeled. The complete labeling need not be visible when the module is installed. The bottom of the module is the recommended location for the label. Labeling shall include:

Appropriate manufacturing and part number identification
Appropriate regulatory compliance labeling
A manufacturing traceability code

The label should also include clear specification of the external port characteristics such as:

Interface standard(s) supported
and/or
Optical wavelength
Required fiber characteristics
Operating data rate
Link length supported

The labeling shall not interfere with the mechanical, thermal or EMI features.

6.3 Optical Interface

Unless specified in the relevant standard, the recommended connectors are: a male MPO connector as specified in IEC 61754-7 (see Figure 6-4) or a dual LC as specified in IEC 61754-20 (see Figure 6-5). The assignment of transmit and receive directions is shown in Figure 6-2 and Figure 6-3.

The four fiber positions on the left as shown in Figure 6-2, with the key up, are used for the optical transmit signals (Lane 1 to 4). The fiber positions on the right are used for the optical receive signals (Lane 4 to 1).

The central four fibers may be physically present.

Two alignment pins are present.

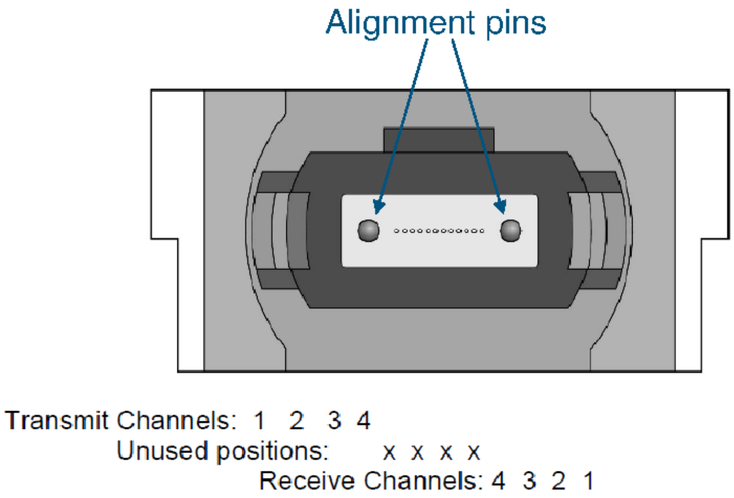

FIGURE 6-2 OPTICAL RECEPTACLE AND LANE ORIENTATION FOR MPO CONNECTOR

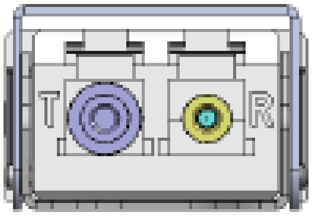

FIGURE 6-3 OPTICAL RECEPTACLE FOR DUAL LC CONNECTOR

6.3.1 MPO Optical Cable Connection

Aligned key (Type B) MPO patch cords should be used to ensure alignment of the signals between the modules. The aligned key patch cord is defined in IEC 61754-7 and shown in Figure 6-4. The optical connector is orientated such that the keying feature of the MPO receptacle is on the top.

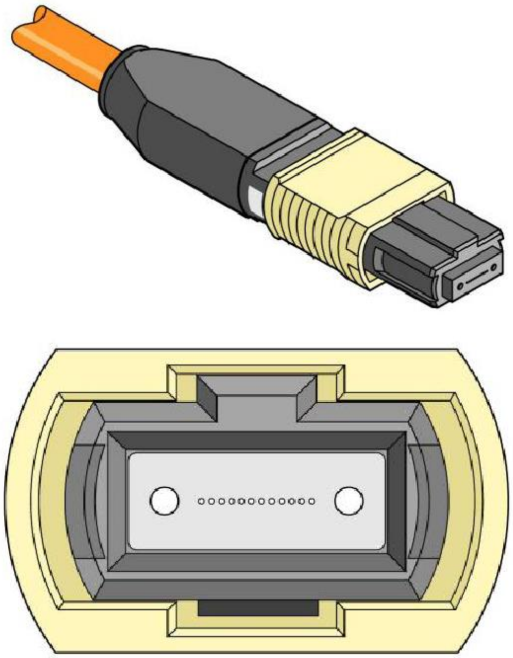

FIGURE 6-4 MPO OPTICAL PATCH CORD

6.3.2 Dual LC Optical Cable Connection

The Dual LC optical connector plug is defined in IEC 61754-20 and also in TIA/EIA-604-10A and is shown in Figure 6-5.

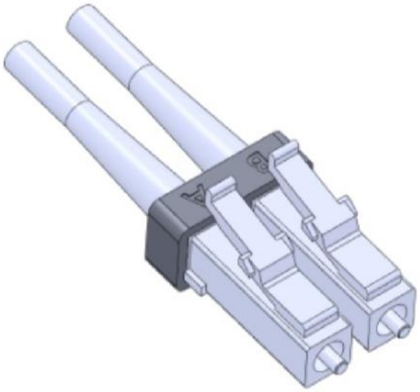

FIGURE 6-5 DUAL LC OPTICAL CONNECTOR PLUG

7 Environmental and Temperature

7.1 Temperature Requirements

The module shall operate within one or more of the case temperatures ranges defined in Table 7-1. The temperature ranges are applicable between 60 m below sea level and 1800 m above sea level, (Ref. Telcordia GR-63-CORE) utilizing the host’s designed airflow.

TABLE 7-1 TEMPERATURE RANGE CLASS OF OPERATION

Class	Case Temperature Range
Standard	0 to 70 ºC
Extended	-5 to 85 ºC
Industrial	-40 to 85 ºC
Custom	Reported by two-wire interface (see SFF-8636)

8 Timing Requirements

A block diagram illustrating the control and status signals between a host system and a QSFP+ module is shown in Figure 8-1. Timing requirements for the signals SCL and SDA are provided in the SFF-8636 specification. Timing requirements for: ResetL, LPMode/TxDis, ModSelL, IntL/RxLOSL signals are provided in this section. In addition, the timing of control and status functions implemented via the two-wire interface are provided.

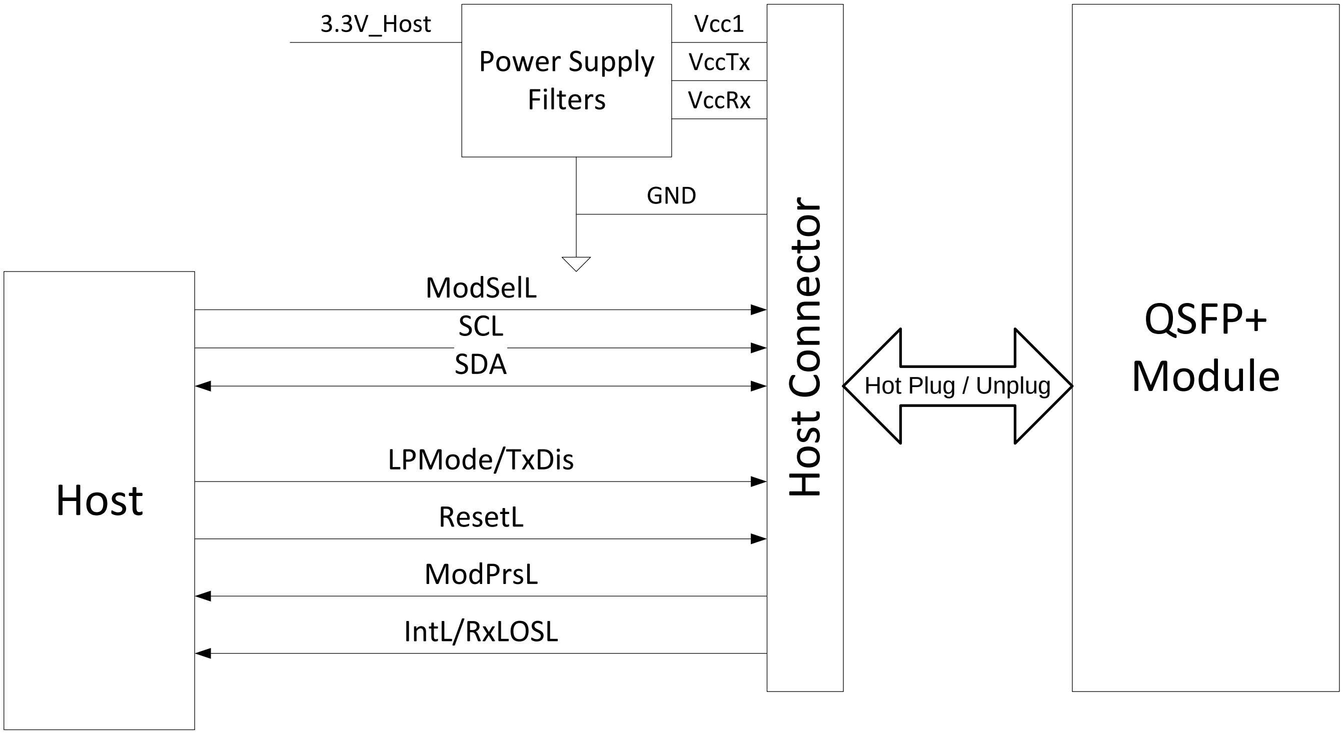

FIGURE 8-1 BLOCK DIAGRAM OF MODULE CONTROL SIGNALS

8.1 Control and Status Timing Requirements

TABLE 8-1 CONTROL AND STATUS TIMING REQUIREMENTS

Parameter	Symbol	Min	Max	Unit	Conditions	Notes
Initialization time	t_init		2	s	Time from power on or hot plug until the module is fully functional. This time applies to Power Class 2 or higher modules when LPMode is pulled low by the host, and to all Power Class 1 modules.	2,3, 6
Reset Init Assert Time	t_reset_init	10	-	μs	Host is required to provide a reset pulse of at least the minimum value for the module to guarantee a reset sequence. Shorter pulses may reset the module depending on implementation.	
Serial Bus Hardware Ready Time	t_serial		2	s	Time from power on until the module responds to data transmission over the two-wire serial bus.	2
Monitor Data Ready Time	t_data		2	s	Time from power on to Data_Not_Ready, Byte 2 bit 0, cleared to 0 and IntL output pulled low.	2
Reset Assert Time	t_reset		2	s	Time from a rising edge on the ResetL input until the module is fully functional.	3
LPMode/TxDis mode change time	t_LPMode/TxDis		100	ms	Time to change between LPMode and TxDis modes of the dual-mode signal LPMode/TxDis	
LPMode Assert Time	ton_LPMode		100	ms	Time from when the host releases LPMode to high until module power consumption reaches Power Class 1.	
LPMode Deassert Time	toff_LPMode		300	ms	Time from when the host pulls LPMode low until the module is fully functional.	3, 5
IntL/RxLOSL mode change time	t_IntL/RxLOSL		100	ms	Time to change between IntL and RxLOSL modes of the dual-mode signal IntL/RxLOSL.	
IntL Assert Time	ton_IntL		200	ms	Time from occurrence of condition triggering an interrupt until IntL is low.	
IntL Deassert Time	toff_IntL		500	μs	Time from clear on read operation of associated flag until module releases IntL to high. This includes the time to clear Rx LOS, Tx Fault and other flag bits.	4
RxLOSL Assert Time (Optional Fast Mode)	ton_f_LOS		1	ms	Optional fast mode is advertised via the management interface (SFF-8636). Time from optical loss of signal to RxLOSL signal pulled low by the module.	

Parameter	Symbol	Min	Max	Unit	Conditions	Notes
RxLOSL Deassert Time (Optional Fast Mode)	toff_f_LOS		3	ms	Optional fast mode is advertised via the management interface (SFF-8636). Time from optical signal above the LOS deassert threshold to when the module releases the RxLOSL signal to high.	
Rx LOS Assert Time	ton_LOS		100	ms	Time from Rx optical signal loss to Rx LOS bit set to 1 and IntL pulled low by the module.	
Tx Fault Assert Time	ton_Txfault		200	ms	Time from Tx Fault state to Tx Fault bit set to 1 and IntL pulled low by the module.	
Flag Assert Time	ton_flag		200	ms	Time from condition triggering flag to associated flag bit set to 1 and IntL pulled low by the module.	
Mask Assert Time	ton_mask		100	ms	Time from mask bit set to 1 until the module is prevented from pulling IntL low when the associated flag is set high.	1
Mask Deassert Time	toff_mask		100	ms	Time from mask bit cleared to 0 until module is enabled to pull IntL low when the associated flag is set high.	1
Application or Rate Select Change Time	t_ratesel		100	ms	Time from change of Application Select Byte or Rate Select bit until module is in conformance with the appropriate specifications for the new application or rate.	1,7
Power_override or Power_set Assert Time	ton_Pdown		100	ms	Time from Power_override or Power_Set bit set to 1 until module power consumption reaches Power Class 1.	1
Power_override or Power_set Deassert Time	toff_Pdown		300	ms	Time from Power_override or Power_Set bit cleared to 0 until the module is fully functional.	1

Note 1: Measured from rising edge of SDA during STOP sequence of write transaction.

Note 2: Power on is defined as the instant when supply voltages reach and remain at or above the minimum level specified in Table 5-6.

Note 3: Fully functional is defined as the module being ready to transmit and receive valid signals and all management interface data, including monitors, being valid. It is indicated after Reset or hot plug by the module releasing IntL to high after the host has read a 0 from the Data_Not_Ready flag bit.

Note 4: Measured from rising edge of SDA during STOP sequence of read transaction.

Note 5: Does not apply to Power Class 1 modules.

Note 6: For some modules this limit is overridden via the management interface, SFF-8636, or by custom product specifications.

Note 7: For Fibre Channel speed negotiation, the 100 ms limit is too slow. See the relevant standard for details of the timing requirements.

8.2 Squelch and Tx/Rx Disable Assert, Deassert and Enable/Disable Timing

Table 8-2 lists the required timing performance for assert, deassert, enable and disable of the Tx Squelch, Rx Squelch, Tx Disable and Rx Output Disable functions.

TABLE 8-2 QSFP+ SQUELCH AND TX/RX DISABLE TIMING

Parameter	Symbol	Max	Unit	Conditions	Note
Rx Squelch Assert Time	ton_Rxsq	15	ms	Time from loss of Rx input signal until the squelched output condition is reached. See 5.5.1.	
Rx Squelch Deassert Time	toff_Rxsq	15	ms	Time from resumption of Rx input signals until normal Rx output condition is reached. See 5.5.1.	
Tx Squelch Assert Time	ton_Txsq	400	ms	Time from loss of Tx input signal until the squelched output condition is reached. See 5.5.2.	
Tx Squelch Deassert Time	toff_Txsq	400	ms	Time from resumption of Tx input signals until normal Tx output condition is reached. See 5.5.2.	
Tx Disable Assert Time	ton_TxDis	100	ms	Time from Tx Disable bit set to 1 until optical output falls below 10% of nominal.	1
Tx Disable Deassert Time	toff_TxDis	400	ms	Time from Tx Disable bit cleared to 0 until optical output rises above 90% of nominal.	1
Tx Disable Assert Time (Optional Fast Mode)	ton_f_TxDis	3	ms	Optional fast mode is advertised via the management interface (SFF-8636). Time from TxDis signal high to the optical output reaching the disabled level.	
Tx Disable Deassert Time (Optional Fast Mode)	Toff_f_TxDis	10	ms	Optional fast mode is advertised via the management interface (SFF-8636). Time from TxDis signal low to the optical output reaching the enabled level.	
Rx Output Disable Assert Time	ton_RxDis	100	ms	Time from Rx Output Disable bit set to 1 until Rx output falls below 10% of nominal.	1
Rx Output Disable Deassert Time	toff_RxDis	100	ms	Time from Rx Output Disable bit cleared to 0 until Rx output rises above 90% of nominal.	1
Squelch Disable Assert Time	ton_sqDIS	100	ms	This applies to Rx and Tx Squelch and is the time from bit cleared to 0 until squelch functionality is disabled.	1
Squelch Disable Deassert Time	toff_RxDis	100	ms	This applies to Rx and Tx Squelch and is the time from bit set to 1 until squelch functionality is enabled.	1
Note 1: Measured from rising edge of SDA during STOP sequence of write transaction.					

8.3 QSFP Management Interface Timing Parameters

The ModSelL pad and the aborted sequence behavior are specific to QSFP/QSFP+/QSFP+ modules. Other timing for the SCL and SDA lines can be found in SFF-8636.

TABLE 8-3 QSFP MANAGEMENT INTERFACE TIMING PARAMETERS

Parameter	Symbol	Min	Max	Unit	Conditions
ModSelL Setup Time (Note 1)	Host_select_setup	2		ms	Setup time on the select lines before start of a host initiated serial bus sequence
ModSelL Hold Time (Note 1)	Host_select_hold	10		us	Delay from completion of a serial bus sequence to ModSelL rising edge.
Aborted sequence – bus release	Deselect_Abort		2	ms	Delay from a host setting ModSelL to high (at any point in a bus sequence) to the QSFP module releasing SCL and SDA

Note 1: ModeSelL Setup and Hold times are requirements on the host system.

Appendix A. Two-wire Interface Timing

A.1 Timing Diagram

The diagram in Figure A-1 illustrates the timing parameters for the two-wire interface clock (SCL) and data (SDA) signals.

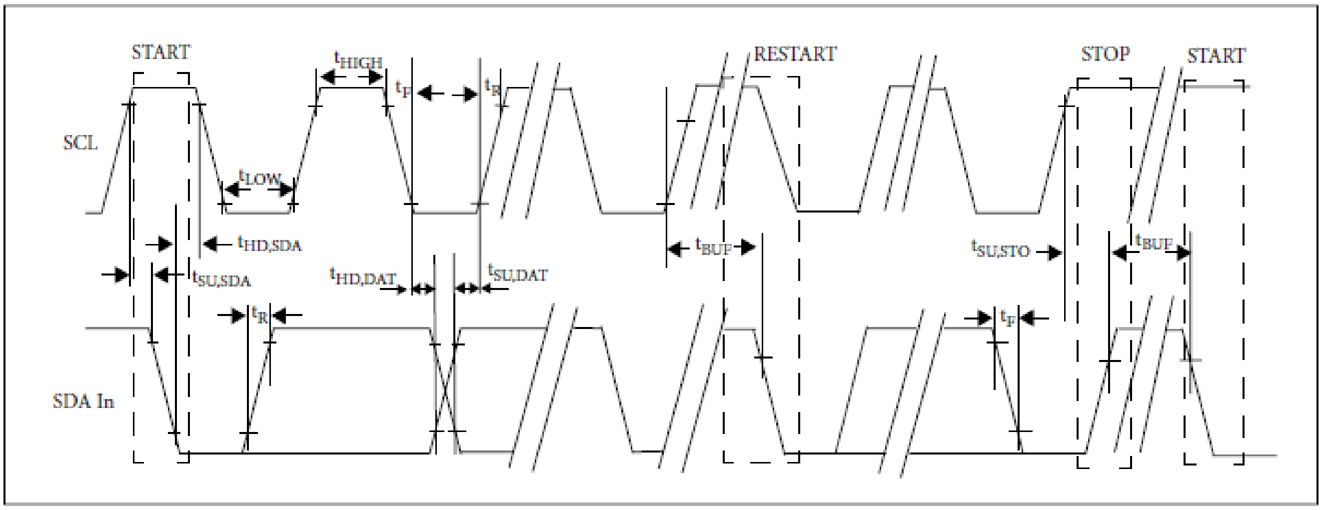

FIGURE A-1 TWO-WIRE INTERFACE TIMING DIAGRAM

A.2 Timing Parameters

The minimum and maximum limits for the timing parameters are provided in Table A-1 for a clock (SCL) frequency of up to 400 kHz.

TABLE A-1 MANAGEMENT INTERFACE TIMING PARAMETERS

Parameter	Symbol	Min	Max	Unit	Conditions
Clock Frequency	fSCL	0	400	kHz	
Clock Pulse Width Low	tLOW	1.3		us	
Clock Pulse Width High	tHIGH	0.6		us	
Time bus free before new transmission can start	tBUF	20		us	Between STOP and START and between ACK and Restart
START Hold Time	tHD.STA	0.6		us	
START Set-up Time	tSU.STA	0.6		us	
Data in Hold Time	tHD.DAT	0		us	
Data in Set-up Time	tSU.DAT	0.1		us	
Input Rise Time (400 kHz)	tR.400		300	ns	From (VIL, MAX-0.15) to (VIH, MIN +0.15)
Input Fall Time (400 kHz)	tF.400		300	ns	From (VIH, MIN + 0.15) to (VIL, MAX - 0.15)
STOP Set-up Time	tSU.STO	0.6		us	
Clock Holdoff Time (Clock Stretching)	T_clock_hold		500	us	Maximum time the module may hold SCL low before completing a read or write operation

A.3 Timing for non-volatile memory writes

Table A-2 provides requirements for the non-volatile memory in the module. For SFF-8636 implementations this timing applies to page 02h, the user writeable memory page.

TABLE A-2 NON-VOLATILE MEMORY SPECIFICATION

Parameter	Symbol	Min	Max	Unit	Conditions
Complete Single or Sequential Write	tWR		40	ms	Complete a sequential write of up to four bytes.
Endurance (Write Cycles)		50,000		cycles	70 °C

END OF DOCUMENT